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THESIS

THE VLSI IMPLEMENTATION OF A GaAs GIC SWITCHED CAPACITOR FILTER

by

Harry G. Oldland III

June 1997

Thesis Advisor: Sherif N. Michael

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REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE June 1997	3. REPORT TYPE AND DATES COVERED Master's Thesis

4. TITLE AND SUBTITLE THE VLSI IMPLEMENTATION OF A GaAs GIC SWITCHED CAPACITOR FILTER	5. FUNDING NUMBERS
6. AUTHOR(S) Oldland, Harry G.	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey CA 93943-5000	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.	12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

Presented is the initial step for the eventual implementation of a programmable GIC switched capacitor filter in a GaAs process. This thesis is the initial engineering effort in the accomplishment of this goal. The focus of this thesis is to design, fabricate, and test all necessary components for the construction of a GIC switched capacitor filter. All components will be stand alone so that future testing of each component may be accomplished. VLSI implementation will be accomplished using the Magic Cad package and the Vitesse HGaAs3 fabrication process. The simulation of the components will be accomplished using HSpice.

14. SUBJECT TERMS *GaAs, switched capacitor, GIC, VLSI, HSpice, Magic, Cadence.	15. NUMBER OF PAGES * 135
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18 298-102

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THE VLSI IMPLEMENTATION OF A GaAs GIC SWITCHED CAPACITOR FILTER

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 1997

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ABSTRACT

Presented is the initial step for the eventual implementation of a programmable Generalized Immitance Converter (GIC) switched capacitor filter in a GaAs process. This thesis is the initial engineering effort in the accomplishment of this goal. The focus of this thesis is to design, fabricate and test of all necessary components for the construction of a GIC switched capacitor filter. All components will be stand alone so that future testing of each component may be accomplished. VLSI implementation will be accomplished using the Magic Cad package and the Vitesse HGaAs3 fabrication process. The simulation of the components will be accomplished using HSpice.

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I. INTRODUCTION

A. BACKGROUND

Integrated Circuit (IC) technology has advanced tremendously in the last 20 years. With advances in crystal growth techniques, implantation technology and IC wafer lithography, the IC chip is undoubtedly a mainstay and driving force in today's market place. Most advances have focused on digital silicon technology. However, the inherent capability of silicon is quickly reaching its limit. Gallium arsenide (GaAs) technology possess the clear potential to provide the speed that is quickly becoming the requirement of today's electronic devices. Until recently GaAs devices were commonly used only in microwave circuits. With the explosion of hand held high frequency communication devices GaAs has seen a substantial increase in its role within the IC world. Along with this increased application has come a renewed interest in GaAs application in general. One such application is in analog filters.

Analog filters are common in everyday devices. The need for smaller devices has necessitated the production of entire systems aboard a single IC. The difficulty with producing analog filters on ICs is the need for resistors. Resistors are virtually impossible to fabricate accurately on an IC using any semiconductor process. This difficulty fueled the already great interest in digital filters and appeared to be the death of analog filters. One solution for this is analog sampled data circuits which uses periodic sampling techniques. Periodic sampling provides the engineer the ability to produce very accurate resistors on the IC. The benefit of analog filters is that unlike their digital filter

counterpart, there is no delay introduced due to analog to digital processing and digital to analog conversion. Analog filters therefore provide a substantial reduction in time delay for the filtering of a given signal, as well as a large reduction in system complexity.

B. THESIS ORGANIZATION

The purpose of this thesis is to initiate research into the viability of using GaAs for the construction of a digitally programmable, switched capacitor General Immittance Converter (GIC) filter. Neither the switched capacitors nor the GIC filter are new ideas. However, what is new is combining the two using the GaAs technology in order to realize a high frequency, high bandwidth filter as a stand alone device.

Chapter II provides the background on filters and the GIC filter in detail. Although it is not the intent of this thesis to provide analysis of the GIC filter it is a goal of this thesis to initiate research that will lead to its construction from the components developed in this research. Additionally, it is necessary to study the GIC filter to understand the subsequent chapters.

Chapter III provides a background understanding of GaAs technology. This chapter concludes with a discussion of the Vitesse HGaAs3 process used in this research.

Chapter IV is a detailed discussion of the basic GaAs devices used in this research. It is not the purpose of this chapter to discuss circuits but merely provide the discussion on how the basic working components for circuits are constructed.

Chapter V provides a detailed discussion of switched capacitor networks. Switched capacitors are discussed in general and the bi-linear resistor used in this research is presented.

Chapter VI is the presentation of operational amplifiers. Much of this chapter was taken from earlier research by Carson (1995) and is presented here for design understanding and research continuity.

Chapter VII provides the background on the layout and fabrication efforts of this research. This is followed by Chapter VIII which is the conclusions and recommendations.

Appendix A is a compilation of all referenced VLSI layouts which were generated for this research. Appendix B is the HSpice code and referenced data produced in the course of this research.

II. GENERALIZED IMMITANCE CONVERTER (GIC) FILTER BASICS

A. FILTER BASICS

The purpose of a filter in electrical engineering applications is to pass and or amplify signals at certain frequencies and to block and or attenuate signals at other frequencies. There are four general ways to describe a type of filter; lowpass, highpass, bandpass and notch. These descriptions are all used to describe the frequency output of a

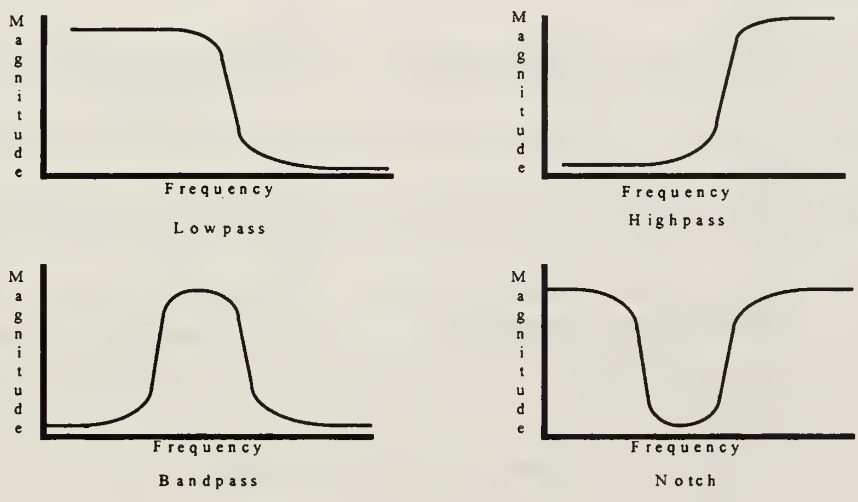


Figure 2.1 Four Basic Filter Types

filter. Figure 2.1 is a graphical depiction of these four filter types. It is typically desirable for the designer to achieve a near ideal frequency response from a given filter. As seen in Figure 2.2 an ideal filter would pass only the desired frequencies and fully attenuate unwanted frequencies. Ideal filters are not an achievable prospect due to the natural limitation of electronic components and circuit designs. Since ideal filters are not obtainable, designers will emphasize either the slop of attenuation, the flatness of the

amplification or the phase response of the filter. Many times the designer must optimize a combination of these design parameters due system requirements. Filters and combinations of filters are designed in an effort to achieve a specified frequency output of a specific amplitude at a specific phase. The more exacting the requirement of the filter the greater its complexity.

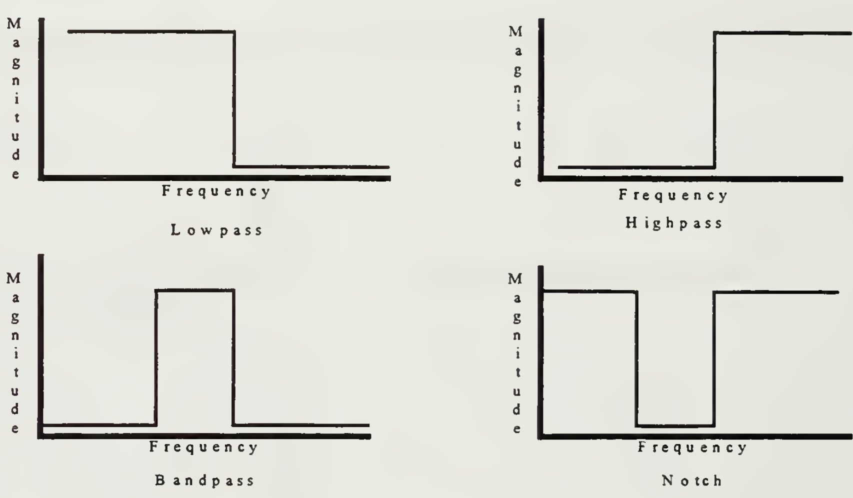


Figure 2.2 Four Basic Ideal Filters

One common parameter used to describe the performance of a filter is its quality factor or as commonly referred "Q factor". The Q factor of a filter is the inverse of the normalized bandwidth of a filter. Normalization is calculated using the half power (3db) point of the filter. Figure 2.3 is a graphical depiction of Q-factor calculation and Equation 2.1 demonstrates the Q factor calculation.

$$Q = \frac{f_0}{f_1 - f_2} \qquad \text{(Eq 2.1)}$$

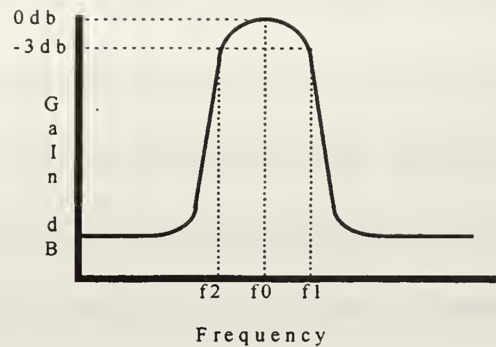


Figure 2.3 Quality Factor For Bandpass Filter

Since filters are concerned with their effect on frequencies, they are described mathematically in the frequency domain through the use of Laplace transforms. The order of the equation used to describe a filter is referred to as the order of the filter. The second order (Bi-Quadratic) transfer functions for the four types of filters are listed in Table 2.1, where ω_p is the pole frequency and Q_p is the pole quality factor.

Filter Topology	Transfer Function
Lowpass	$H(s) = \dfrac{2\omega_p^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p}$
Highpass	$H(s) = \dfrac{2s^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p}$
Bandpass	$H(s) = \dfrac{\dfrac{2\omega_p}{Q_p}s}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p}$
Notch	$H(s) = \dfrac{s^2 + \omega_n^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p}$

Table 2.1 Transfer Functions for Bi-Quadratic Filter

Another way to describe a filter is by the way it is constructed. There are two approaches to filter construction; active and passive. Passive filters use a network of resistors, inductors and capacitors which are connected in order to achieve a specific frequency output. They do not require the input of additional power. Passive filters can, at best, achieve an amplification of one and therefore concentrate their effect on attenuating the undesired frequencies. Due to the difficulty of fabricating high quality accurate inductors on chip, passive RLC filters are an undesirable engineering approach. Active filters are constructed by using resistors, capacitors and operational amplifiers. Operational amplifiers enable the designer to overcome the shortfall of inductors as well as to provide additional signal amplification.

B. THE GIC FILTER

There are numerous active filter configurations which are routinely used. The Bessel-Thompson, Butterworth, Caur and Chebyshev are some of the most popular filter designs in use. These filters all possess certain characteristics (sensitivities) which can be exploited by the engineer for specific applications. The quality of a filter is dependent on the variation of all the components and factors affecting the signal. The variation of component fabrication, temperature, humidity, aging and parasitic capacitance all will affect the performance of a specific filter. It is the extent to which these parameters affect the filter performance that is referred to as a filters sensitivity. Filter sensitivity analysis alone is of little value unless compared to actual operating parameters or compared to a

filter of another design. Sensitivity calculations are also used to optimize filter design as well as minimizing filter complexity.

The General Immittance Converter (GIC) filter is another popular filter configuration which is substantially less sensitive than any of the aforementioned filter designs. This design has been referred to by many as the best filter design available. Its relative complexity at lower order filters is to some a counter argument to its performance. Figure 2.4 depicts the general filter design of the GIC filter.

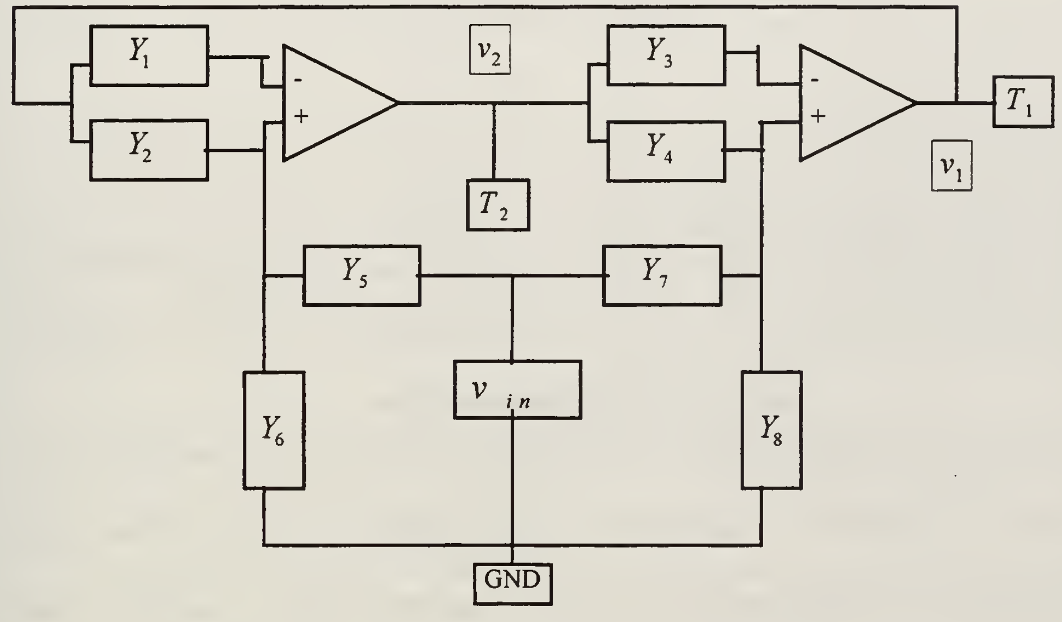


Figure 2.4 The General Immittance Converter Filter

The output of this filter is taken from node T1 for highpass and bandpass filters and from node T2 for lowpass and notch filters. Analysis of this filter is done using admittance vice impedance because the mathematics is simplified. Equation 2.2 and Equation 2.3 depict the voltage transfer functions. Note that the denominators of these

equations are equal. By substituting the values found in Table 2.2 into these equations one is able to evaluate these equation for specific filter types where G is the admittance of the resistance, C is the capacitance, and Q_p is the pole quality factor. Table 2.3 is a table of the derivation of this process for second order GIC filters.

$$T_1 = \frac{v_1}{v_{in}} = \frac{Y_1Y_4Y_5 + Y_3Y_7(Y_2 + Y_6) - Y_3Y_5Y_8}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)} \quad \text{(Eq 2.2)}$$

$$T_2 = \frac{v_2}{v_{in}} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)} \quad \text{(Eq 2.3)}$$

Filter Type	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8
Lowpass	G	C	C+G/Q_P	G	G	0	0	G
Highpass	G	G	C	G	0	G	C	G/Q_P
Bandpass	G	G	C	G	0	G	G/Q_P	C
Notch	G	G	C	G	G	0	C	G/Q_P

Table 2.2 GIC Filter Admittance Values

By using the equations listed in Table 2.3, construction of a second order GIC filter can be accomplished in the following manner. After the type of filter to be constructed has been determined, the first major engineering step to consider is what value of Q should be used. Recall from Eq 2.1 that the value of Q will determine the sharpness or slope of the filter. The next step is to select a value for G (which is equal to 1/R) or C. The corner frequency for the filter to be built is dependent on the product of the admittance's of the resistor and capacitors. As can be seen in Table 2.2 the value for G and C are used multiple times. Note that some admittance values are zero. With this completed the last step is to determine the value of the component not previously

selected. This is accomplished by using Eq. 2.4 to find C if G is previously determined and Eq 2.5 to find G if C is previously determined, where ω_p is the critical frequency for the filter being constructed and R is the resistance chosen when selecting G. At this point all necessary components have been determined and the filter design is complete.

Filter Topology	Transfer Function (with discrete values)	Transfer Function
Lowpass	$T_2 = \dfrac{2\dfrac{G^2}{C^2}}{s^2 + \dfrac{Gs}{CQ_p} + \dfrac{G^2}{C^2}}$	$T_{2=} \dfrac{2\omega_p^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Highpass	$T_1 = \dfrac{2s^2}{s^2 + \dfrac{Gs}{CQ_p} + \dfrac{G^2}{C^2}}$	$T_{1=} \dfrac{2s^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Bandpass	$T_1 = \dfrac{2\dfrac{sG^2}{CQ_p}}{s^2 + \dfrac{Gs}{CQ_p} + \dfrac{G^2}{C^2}}$	$T_{1=} \dfrac{2\dfrac{\omega_p}{Q_p}s}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Notch	$T_2 = \dfrac{s^2 + \left(\dfrac{G^2}{C^2} + \dfrac{G^2}{C^2 Q_p}\right)}{s^2 + \dfrac{Gs}{CQ_p} + \dfrac{G^2}{C^2}}$	$T_2 = \dfrac{s^2 + \omega_n^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$

Table 2.3 Transfer Functions for the GIC Filter

$$C = \frac{1}{\omega_p R} \qquad \text{(Eq 2.4)}$$

$$R = \frac{1}{\omega_p C} \qquad \text{(Eq 2.5)}$$

It is the purpose of this research to ultimately construct the necessary components in order to implement a GIC filter using gallium arsenide (GaAs) technology. This

technology promises to provide filters possessing much higher operating frequencies and greater bandwidth. In this chapter a brief overview of the GIC filter was presented so that the reader may have a better understanding of how the subsequent chapters apply to the ultimate goal of this research.

The next chapter discusses the characteristics and advantages of GaAs. The Vitesse HGaAs3 process which is used in this research is discussed in detail.

III. GALLIUM ARSENIDE BASICS

A. HISTORY OF GALLIUM ARSENIDE

Silicon integrated circuit (IC) chips are clearly the dominant form of semiconductors at this time and for the foreseeable future. Ease of production, widely available materials and a large production base makes silicon the material of choice for the vast majority of applications. However, as both analog and digital systems demand greater speeds, silicon technology has difficulty fulfilling the requirements. GaAs technology makes a viable and growing alternative to fulfill the silicon shortfall niche.

GaAs chip technology was first introduced in 1966 with the production of the first GaAs MESFET by Carver Mead at California Technology Institute. The first GaAs MESFETS for solid state amplifiers were not produced commercially until 1973 and were used almost exclusively for digital IC circuits. According to Notes (1996), GaAs applications have since grown steadily accounting for $330 million in sales in 1993 and is projected to reach sales of $1.8 billion by the year 2000. However, this still only constitutes about 2% of the IC chip market. The recent explosion in the wireless communications industry has been a boom to the GaAs industry. The vast majority of GaAs production has focused on this market which requires IC chips capable of operating at very high frequencies (GHz). Relative to silicon, GaAs production technology is still in its infancy. This situation can be expected to improve as industry demands more capable technology at better prices.

B. SEMICONDUCTORS

Gallium and arsenic when combined, form a stable crystal lattice which has current carrying properties between that of a conductor and insulator. The gallium has three electrons in its outer most shell while arsenic has five electrons in its outer most shell. Both atoms have the tendency to hold eight electrons in their outer most shell. When combined a crystal lattice structure is formed. The two atoms then share each others electrons to complete their outer shell capacity. The bonds formed between these outer electrons are called covalent bonds. If sufficient energy is introduced into the crystal lattice it is possible to break an electron free from its parent atom. This then creates a hole in the lattice structure. A hole is defined as the absence of an electron. The creation of a hole places the parent atom in an electrically positive state. The recombination of electrons from other atoms with an atom with a hole will return the atom to equilibrium. After recombination energy is freed up to permit another electron to be freed from its parent atom. As long as energy is continued to be applied this process will continue. It is the application of energy to the GaAs lattice structure which provides it the capability to conduct.

By adding specific impurities into the GaAs lattice structure the conductivity of the GaAs can be modified to achieve specific results. Impurities are added to either create a n-type area or p-type area. The n-type region is one where there is a greater availability of electrons. The p-type region is one where there is a greater availability of holes. GaAs, as will be explained in the next section, lends itself to the formation of n-type materials. Silicon is typically used to produce n-type GaAs. Adding silicon to the GaAs substance

creates an inbalance in the outer shell where there is an excess number of electrons. The excess electrons will not be covalently bonded into the lattice structure. In this situation the electron is referred to as the majority carrier. The conductive properties of GaAs are increased when a dopent is added to its lattice structure.

C. GALLIUM ARSENIDE PROPERTIES

As was mentioned above, GaAs is formed by combining gallium (a type III material) and arsenic (a type V material). This combination is referred to as a III-V material. There are other III-V materials (i.e., InAs, InP, InSb) that are being researched as alternative semiconductor materials. The major advantage of GaAs is its high electron mobility coefficient ($\mu_n = 8500 cm^2 / V-s$), which is over six times faster than the silicon electron mobility coefficient ($\mu_n = 1350 cm^2 / V-s$). The higher electron mobility allows electrons in GaAs to travel faster than its counterpart in silicon. This permits greater currents at higher frequencies than can be achieved in silicon. This greater current then allows greater gain to be achieved by GaAs devices at higher frequencies. To better demonstrate this, Eq 3.1 shows the effect of μ_n on the electron diffusion coefficient,

$$D_n = \mu_n kT / q \qquad \text{(Eq 3.1)}$$

where k is Boltzmann's constant, T is the effective temperature and q is the charge of an electron. The electron diffusion coefficient D_n of a material is the net motion of electrons to areas of decreasing electron concentration within a semiconductor device. D_n for GaAs is 220 cm^2/s and for silicon is 100 cm^2/s. D_p which is the hole diffusion coefficient is the net motion of holes to areas of decreasing hole concentration within a semiconductor

device. D_p for GaAs is 10 cm^2/s and for silicon is 50 cm^2/s. Both D_n and D_p, as can be seen in Eq 3.2, have a direct impact on the total current in a forward biased junction. Derivation of this equation is covered in Streetman (1995), where q is the charge of an electron, A is the cross sectional area of the junction, L_p is the diffusion length for holes, L_n is the diffusion length for electrons, p_n is the hole concentration in the N side of the PN junction and n_p is the electron concentration in the P side of the PN junction.

$$I = qA\{(\frac{D_p}{L_p} p_n) + (\frac{D_n}{L_n} n_p)\}e^{qV/kT} \qquad \text{(Eq 3.2)}$$

The diffusion coefficient greatly affects what types of devices are able to be constructed. Since GaAs possess a high μ_n and thus a high D_n, n-channel devices are very capable relative to their silicon counterpart. However, since GaAs μ_p is relatively low and thus makes for a low D_p, GaAs p-channel devices are extremely poor devices. The p-channel devices are so poor that until recently, they were not used. This limitation requires the GaAs designer to use only n-channel devices. This shortfall does not prevent GaAs from being used to achieve any required analog or digital circuits but does require more transistors per logic gate as compared to silicon CMOS designs. It should be mentioned that Motorola has recently introduced a GaAs complementary process which will focus on digital circuit implementation. More discussion on specific devices and their designs will be presented in later chapters.

Another characteristic found in GaAs is its semi-insulating property. Pure undoped GaAs is a semi-insulating material. The advantage of this is that chips fabricated

on a GaAs substrate do not require the added insulating layer as is required in silicon fabrication. This allows GaAs designs to use fewer fabrication steps relative to silicon devices.

There are some additional advantages to GaAs. First, GaAs circuits exhibit very high tolerance to total dose radiation effects. Secondly, GaAs devices possess very low parasitic capacitance. These advantages coupled with the speed provided by the electron mobility enable GaAs devices to fulfill many of the requirements for microwave applications, space applications, as well as other emerging technology.

GaAs devices are of course no panacea for the engineer. As with most things in life you do not get something for nothing and this is also the case with GaAs. There are drawbacks of GaAs which prevent it from replacing silicon entirely. The most predominant drawback is as a result of the poor μ_p for GaAs. This factor prevents the effective construction of p-channel devices. The net effect of this complicates the construction of logic gates relative to the silicon CMOS process. Additionally, this results in fewer gates per unit area, making GaAs use a greater portion of the chip area to achieve the same number of gates. Digital GaAs gates also have relatively low voltage swings requiring very low noise margins. Another difficulty encountered with GaAs technology is that it is still a relatively new material. Unlike silicon, which has been in development for more than 50 years, GaAs has really been around for only 35 years. This, coupled with the relative brittle nature of GaAs, causes smaller chip yields per wafer as compared to silicon. This, in turn increases the cost of production of GaAs chips. Although GaAs

devices exhibit greater gain at higher frequencies, their gain is significantly lower than that of silicon devices at lower frequencies.

As can be seen from the discussion above GaAs has both capabilities and drawbacks when being considered. The applications of GaAs circuits will clearly grow in the future as the need for faster logic and higher frequency devices emerges. GaAs is best suited for high upper end high frequency applications. Additionally, GaAs has tremendous benefits in applications where radiation is a factor. GaAs will never entirely replace silicon but it can be expected to increase its presence in the market place.

To fully understand and appreciate GaAs device capabilities and limitations it is necessary to present more detailed information on specific devices. In the next chapter each of the major devices used in the GaAs VLSI process will be addressed.

D. VITESSE FABRICATION PROPERTIES

The following section is covered as in Notes (1996). The GaAs fabrication process is very similar to the silicon process in many ways. In fact, once the individual devices have been constructed the routing process is nearly identical. The major GaAs chip producers are Motorola, TriQuint, and Vitesse to name a few. As has been mentioned earlier, the process available for this research is through the MOSIS service which utilizes the Vitesse H-GaAs III 0.8 um process.

Vitesse introduced the H-GaAs I process in 1986. This processes was quickly improved and in 1988 the H-GaAs II process was introduced. Again improvements were made and in 1990 the H-GaAs III process was introduced. It is this process that is to be

used for this research. Vitesse improved their process and in 1995 introduced the H-GaAs IV process. However, MOSIS does not offer the H-GaAs IV through their service at the time of this writing. Additionally, MOSIS only offers the 0.8 um H-GaAs III process and not he 0.6 um. Table 3.1 displays the above mentioned processes and their capabilities.

	H-GaAs I	H-GaAs II	H-GaAs III	H-GaAs IV
Gate (Leff)	1.2 um	0.8 um	0.6 um	0.5 um
Metal 1	2.5/2.5 um	2.0/2.0 um	1.2/1.8 um	1.2/1.0 um
Metal 2	4.0/4.0 um	3.0/3.0 um	1.8/1.8 um	1.2/1.0 um
Metal 3		6.0/6.0 um	3.0/3.0 um	2.2/2.0 um
Metal 4		NA	NA	NA

Table 3.1Vitesse H-GaAs Process Evolution

Of the 13 masks used in the H-GaAs III process the first four are used to produce devices, and the remaining nine are used for routing. Prior to the first mask the GaAs wafer is covered with a SiO_2/Si_3N_4dielectric layer which functions as an implant barrier layer. The first mask is used to create active area regions on the dielectric layer. The second mask is used to define channel implant and gate deposition through a photo resist layer. After the removal of the photo resist, the third mask provides gate definition and an n+ implantation of Si_{29}. The forth mask establishes the ohmic contacts using tungsten followed by a dielectric deposition. At this point in the process, all transistor and diode fabrication has been. The remaining nine masks are used for routing metal and vias

between metal layers. They can also be used for the fabrication of inductors and capacitors.

As was mentioned above, the process of routing is nearly identical to that in the silicon process. Aluminum is used for each of the four metal routing layers and for the construction of vias between metal layers. Between each metal layer a dielectric layer of SiO2 is deposited. Figure 3.1 shows the entire H-GaAs III process, while Figure 3.2 displays the cut away view of the H-GaAs III process used in the creation of a MESFET.

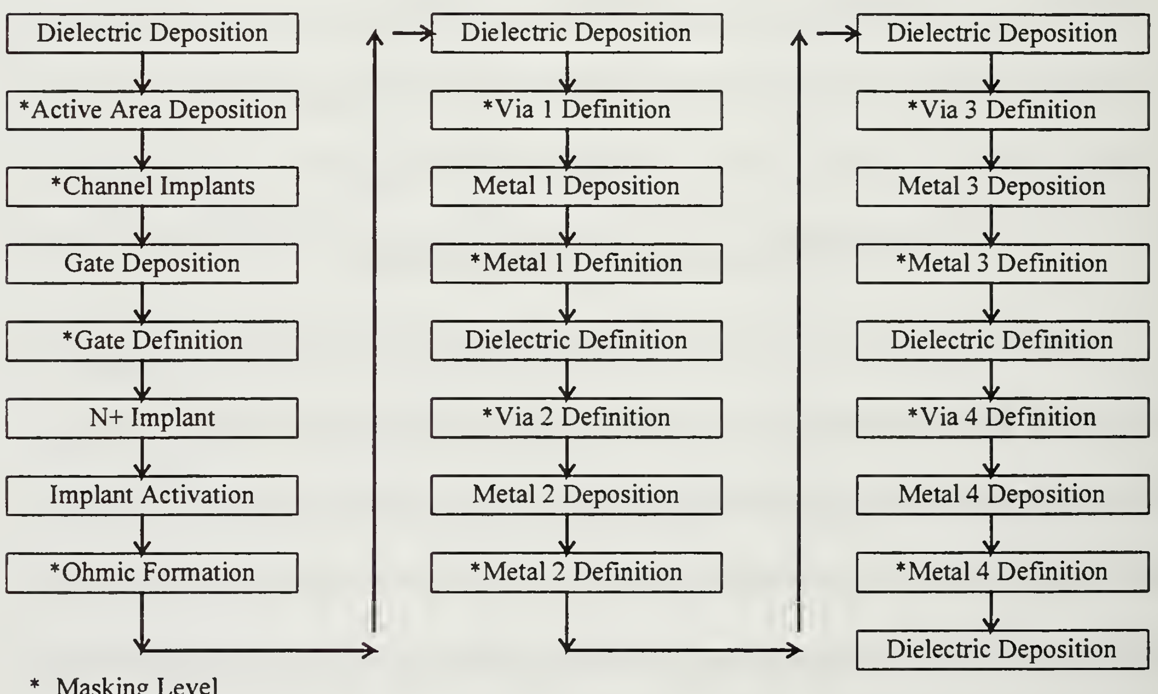


Figure 3.1 Vitesse H-GaAs III Process Sequence

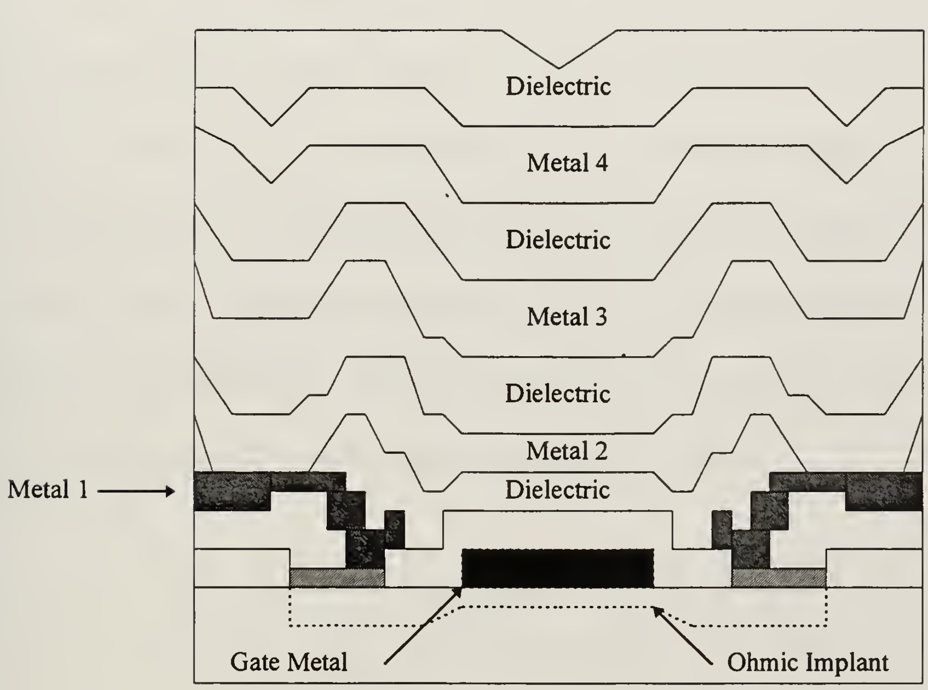


Figure 3.2 H-GaAs III MESFET Process

IV. GALLIUM ARSENIDE DEVICES

A. DIODES

A diode is a device that permits current to flow in only one direction. A diode is a two terminal device . One terminal is called the anode and the other is called the cathode. Current passes from the anode to the cathode. The diode is the most basic non-linear device. There are many applications for diodes. The most common use for a diode is as part of a rectifier circuit used in AC-DC conversion. Diodes are also used as clamps or regulators to limit voltage to a certain range of values. Another application for diodes is as a light emitting diode. Light emitting diodes convert current into light intensity. These are commonly used in fiber optic application. The final major application for diodes is as a solar cell or photodetector. In this application diodes are used to convert light into a flow of electric charge. Figure 4.1 depict the symbol for a diode.

Figure 4.1 Symbol for Diode

1. Diode Operation

An ideal diode is a nonlinear device. The ideal diode would function in the following manner. Any time the cathode becomes more negative than the anode the diode would turn on and function as a short and permit current to flow from the anode to the cathode. Once the voltage difference between the anode and cathode is returned to zero the diode would turn off and function as an open and current would cease to flow. A

diode which is turned off is referred to as being in a reverse biased state. A diode which is turned on is referred to as being in a forward biased state. Figure 4.2 depicts the performance of an ideal diode.

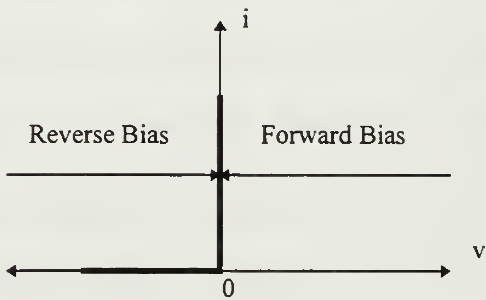


Figure 4.2 Ideal Diode Performance

Real diodes are, as was mentioned earlier, nonlinear devices. Current will begin flowing across the diode upon reaching a forward bias condition, however current flow will increase gradually. At a certain voltage difference, typically around 0.7V, the diode begins functioning as described above.

Silicon diodes are constructed in the form of a PN junction. The Schottkey Barrier Diode (SBD) which is used in GaAs technology, functions in the same manner but has different characteristics and is constructed in a differently. Figure 4.3 depicts the general

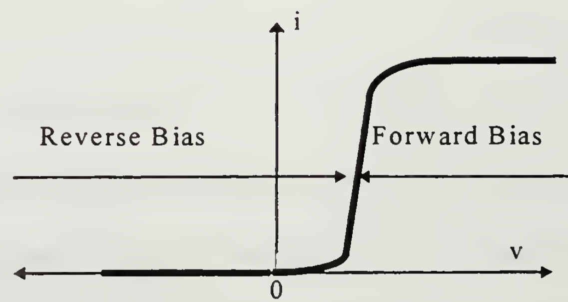


Figure 4.3 Real Diode Performance

i-v characteristics of a SBD. Figure 4.4 shows a cross section of a SBD.

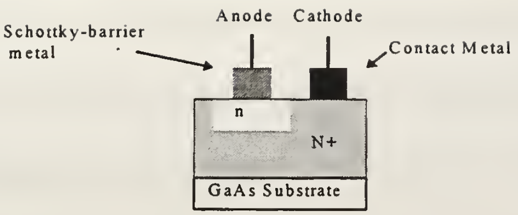


Figure 4.4 Cross Section of a GaAs SBD, Fisher (1995)

The GaAs SBD uses Schottky-barrier metal to form the anode. Schottky-barrier are typically alloys consisting of gold, nickel, titanium, and aluminum. To fully understand the SBD as well as GaAs technology an understanding of the Schottky-barrier is necessary. When a Schottky metal is brought into contact with a semiconductor recombination occurs. The result of this recombination is a change in the electron configuration of the semiconductor. As the recombination occurs, a positive area just beneath the Schottky metal is formed within the semiconductor. Figure 4.5 depicts the Schottky-barrier effect.

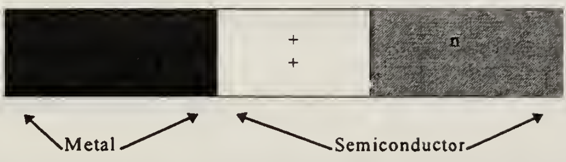


Figure 4.5 Schottky-barrier Effect

The current-voltage characteristics of the SBD and silicon PN junction are very similar. However, the way they perform their function is significantly different. As was previously mentioned, the GaAs strength, is in its high electron mobility. This electron mobility permits the flow of electrons from the semiconductor into the Schottky barrier metal. The electrons are the majority carrier and thus the holes are the minority carriers.

The net result of this, is that their is not a strong migration and therefore not a collection of holes within the bulk area of the semiconductor. The lack of a collection of these minority carriers causes the SBD to transition from forward to a reverse bias much faster than in a silicon PN junction. This results in a breakdown voltages of 0.6 to 0.7 volts for a typical SBD. The exact breakdown voltage can be varied by controlling the amount of n-type doping. This breakdown voltage will effect current capability of the diode. As derived in Streetman (1995), Eq 4.1 shows the SBD current capability for the ideal diode,

$$I_D = I_S[\exp(\frac{qV_{D,i}}{nkT}) - 1] \qquad \text{(Eq 4.1)}$$

where I_s is the saturation current, q is the charge of an electron, n is a constant which ranges from 1 to 1.2, k is Boltzmanns constant, and T is the effective temperature of the device. $V_{D,i}$ is the intrinsic voltage across the diode described in Eq 4.2, where V_D is the voltage across the diode from anode to cathode, and R_S is the series resistance from the combinations of the contacts of the diode. The value for R_S is a function of the fabrication process and is in the best interest of the device to minimize this factor. The voltage across the diode can also be varied slightly by variation of the gate width.

$$V_{D,i} = V_D - I_D R_S \qquad \text{(Eq 4.2)}$$

2. Project Diode Construction

Diodes can also be constructed from a transistor by simply connecting the source and drain together. This technique creates a diode where the gate of the transistor becomes the cathode and the source-drain connection is the anode. This technique was

used in this research. Figure 4.6 shows the cross section of a Metal Semiconductor Field Effect Transistor (MESFET) which has been configured as a diode. Figure 4.7 depicts the symbolic representation of this same technique. Section A of Appendix A shows the VLSI layout of the SBD used in this research.

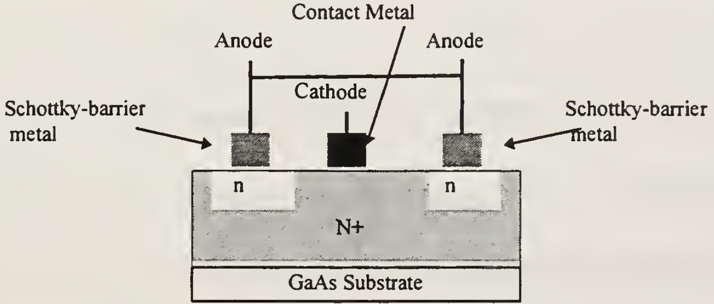


Figure 4.6 Cross Section of a GaAs MESFET

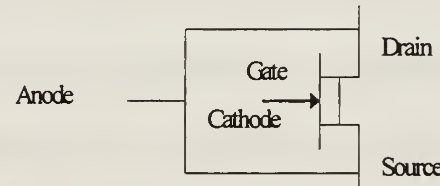


Figure 4.7 Symbolic Depiction of a MESFET as a Diode

3. Project Diode Performance

As was mention at the beginning of this chapter, one of the main purposes of a diode is for voltage level shifting. By using the 0.6 to 0.7 drop across a diode, it can be used to establish bias voltages. This technique was used in designing the operational amplifier and clock amplifier used in this research. These devices will be discussed in greater detail in later chapters. Three diodes were used, each is different in the width and length of the gate, which is the cathode of the diode. Recall that the size of the gate can be varied to provide various voltage drops. The smaller the gate area the more voltage

drop across the diode. Table 4.1 lists the different diodes used in this research and their specifications. The VLSI layout of diode B can be seen in Section A Appendix A.

Diode	Gate Length	Gate Width	Voltage drop
A	1.6 um	2 um	0.8 um
B	3 um	3 um	0.7 um
C	6 um	6 um	0.5 um

Table 4.1 Project SBD Characteristics

B. CAPACITORS

1. Capacitor Operation

Capacitors are widely used in a variety of applications. A capacitor is used as a mean to store charge. All capacitors are basically two conductors separated by an insulator. Unlike resistance values in VLSI fabrication, capacitance values can be made to very exacting values. It is this capability that makes capacitors a relatively desirable device for use by the VLSI designer.

The insulator used is called a dielectric. A dielectric is a nonconducting material which when placed between the conductors of a capacitor increases the capacitance of the capacitor. The degree by which the dielectric increases the capacitance of a capacitor is called the dielectric constant (k). The dielectric constants of some common materials are given in Table 4.2. Equation 4.3 is used to calculate the capacitance of a capacitor, where ε_0 is the permittivity of free space, A is the common area between the two conductors and d is the distance between the two conductors.

$$C = k\frac{\varepsilon_0 A}{d} \qquad \text{(Eq 4.3)}$$

Material	k
Vacuum	1.00000
Air	1.00059
Paper	3.7
Rubber	6.7
Silicon	11.8
GaAs	13.2

Table 4.2 Common Dielectric Constants

As can be seen in Eq 4.3 there are two factors, area of the capacitor and distance between the conductors which the designer will generally have control over when constructing a capacitor. This is especially true when working with VLSI processes where the designer must work with the parameters dictated by the process being used. Capacitance can be increased by either increasing the area or reducing the distance between the conductors. In circuit applications, parallel combinations of capacitors are additive as shown in Eq 4.4. Series combinations of capacitors are equal to the inverse sum of the capacitors in series as shown in Eq 4.5.

$$C_{tot,para} = C_1 + C_2 \qquad \text{(Eq 4.4)}$$

$$\frac{1}{C_{tot,ser}} = \frac{1}{C_1} + \frac{1}{C_2} \qquad \text{(Eq 4.5)}$$

2. Project Capacitor Construction

The size of an effective capacitor in VLSI design has to be chosen carefully, taking into consideration the nature of the technology being used. Of utmost concern, is the amount of parasitic capacitance that exist between the various layers of the chip. As the capacitor in VLSI gets smaller the parasitic capacitance gains in its contribution.

Capacitors must be sized so as to preclude the detrimental effects of parasitic capacitance. Additionally, large capacitors are not possible because of layout size limitations. To construct the capacitor for this research two considerations were necessary. First, an understanding of the capacitances available using the Vitesse process. Second, since the capacitor would be used for a switched capacitor network, an understanding of how capacitors are used in these networks. Switched capacitor networks will be discussed in greater detail in the next chapter. Data concerning the capacitance between each layer of the Vitesse process is available from MOSIS in their home page. Table 4.3 shows the capacitance parameter data used for this research ($aF/um^2=10^{-18}F/10^{-6}m^2$). This data is routinely analyzed by Vitesse after each fabrication run. Examination of other runs shows that there is virtually no change (less than one percent) in the capacitance of one run from another.

Layer	Gate Metal	Metal 1	Metal 2	Metal 3	Metal 4	Units
Gate Metal		59				aF/um^2
Metal 1			30			aF/um^2
Metal 2				21		aF/um^2
Metal 3					19	aF/um^2
Active	5					aF/um^2
Depletion	1826					aF/um^2
Fringe Active	494					aF/um^2

Table 4.3 Vitesse Capacitance Parameters

To construct the capacitor, it is necessary to isolate both conductors from each other as well as be able to access them for termination on a pad on the VLSI chip. Additionally, it is desirable to maximize capacitance as well as minimize the area used on the chip. For these reasons a capacitor was constructed using the gate metal and metal one. In an effort to ease calculations for use in circuits, a capacitor of 0.5 pf was chosen. A capacitor of this size would also ensure limited effects due to parasitic capacitance. To construct a device of this size the capacitance between the gate metal and metal 1 was used to determine the necessary area to achieve the desired capacitor value. The area necessary to achieve this capacitor was found to be 8,473 um^2 resulting from a 92.05x92.05 um square. This area was made by constructing a square of gate metal and metal 1. Two capacitors were made. One capacitor was made to be used in the switched capacitor network which will be discussed in the next chapter. The second capacitor is a stand alone device which can be used for independent testing and evaluation. The VLSI layout of the capacitor constructed for this research can be seen in Section B Appendix A.

C. MESFET

The fundamental building block of electronics for the last 40 years has been the transistor. It is the versatility of the transistor coupled with the increase in VLSI technology which has permitted a growth in the availability of electronic devices. There are various methods using different technologies to construct many different types of transistors. In GaAs the MESFET is the method of transistor fabrication. GaAs MESFETs are more capable at higher frequencies than their silicon Metal Oxide

Semiconductor Field Effect Transistor (MOSFET). Although similar in function they differ in how there channel is formed and how the gate is coupled to the channel. In a MESFET the channel is formed by a thinly doped channel which is controlled by the depletion of the metal semiconductor junction. The gate metal is attached using Schottky barrier metal directly to the channel.

1. MESFET Operation

Currently n-channel GaAs MESFETS are the most commonly available device. A GaAs device has a much higher electron mobility than the hole mobility making an n-channel device preferable and p-channel device relatively useless. The I-V characteristic of a MESFET are very much like its n-channel MOSFET cousin. Figure 4.8 displays the symbol for the depletion channel MESFET and Figure 4.9 demonstrates the symbol for the enhancement channel MESFET. The VLSI layout for a MESFET used in this research is detailed in Section C Appendix A.

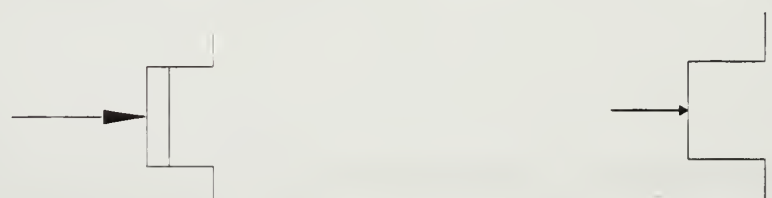


Figure 4. 8 Symbol For DFET **Figure 4.9 Symbol For EFET**

2. Project MESFET Construction

The cross section of a GaAs MESFET is shown in Figure 4.10. The depletion region is formed below the gate when a voltage is applied. The thickness of the depletion

is determined by the intensity of the voltage applied. It is the thickness of this channel which determines the amount of current that can flow from the drain to the source in response to the drain to source voltage. In addition to the greater electron mobility GaAs MESFETs has over silicon MOSFETs, it also use the bulk region to transport electrons instead of the surface as in the case of MOSFETs. Depending on the thickness of the active channel the MESFET may be normally on, which is referred to as a depletion MESFET, or normally off, which is referred to as an enhancement MESFET.

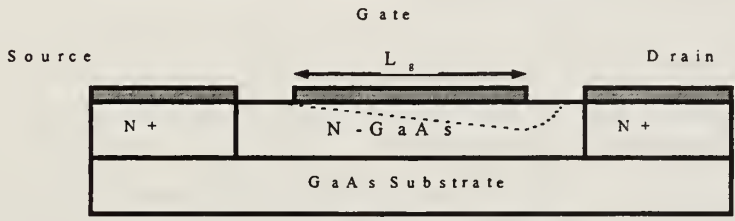


Figure 4.10 Cross Section of a GaAs MESFET, Streetman (1995)

The most commonly used GaAs MESFET is the depletion mode type. The threshold voltage, V_t, is the voltage necessary to apply to the gate of a device, in order to collects a sufficient number of electrons to form a conducting channel. For depletion mode MESFETs V_t can range from -0.5 to -2.5 V. The gate to source voltage, v_{GS}, for depletion mode MESFETs ranges from V_t to a positive voltage approaching the Schottky-barrier voltage of approximately 0.7V. If v_{GS} exceeds the Schottky-barrier voltage an appreciable level of current begins to flow into the channel from the gate. At this point the gate no longer acts as a control for the transistor and begins to provide current to the transistor. The characteristic of gate conduction is a drawback of the MESFET.

Enhancement MESFETs have grown in usage over the last five years. Enhancement MESFETs are constructed by extending the depletion region of the MESFET completely through the channel which when $v_{GS} = 0$ prevents the flow of electrons from the source to the drain. Enhancement MESFETs function more like their silicon MOSFET relatives. In order to create a conduction channel a positive v_{GS} must be applied and thus permits a flow of current from the source to the drain. V_t for enhancement MESFETs ranges from 0.1 to 0.3 V. For this research both depletion type and enhancement type MESFETs were used.

Although GaAs MESFETs are similar in many ways to silicon MOSFETS, the evaluation of the operational characteristics of the GaAs MESFET is not as well developed. Numerous models are used to describe the performance of the MESFET. The most common description of the MESFET drain current, i_d, is shown in Eq 4.6, Eq 4.7, and Eq 4.8 which are derived in Sedra (1991),

CUTOFF

$$i_d = 0 \text{ for } v_{GS} < V_t \qquad \text{(Eq 4.6)}$$

LINEAR

$$i_d = \beta\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right](1 + \lambda v_{DS}) \text{ for } v_{GS} \geq V_t, v_{DS} < v_{GS} - V_t \qquad \text{(Eq 4.7)}$$

SATURATION

$$i_d = \beta\left[(v_{GS} - V_t)^2\right](1 + \lambda v_{DS}) \text{ for } v_{GS} \geq V_t, v_{DS} \geq v_{GS} - V_t \qquad \text{(Eq 4.8)}$$

where the value for the transistor transconductance, β, is as shown in Eq 4.9. The effect

$$\beta = \frac{2\varepsilon_S \mu_n v_{sat} W}{b\left(\mu_n V_{po} + 3v_{sat} L\right)} \qquad \text{(Eq 4.9)}$$

of β on i_d can easily be seen as a significant contribution to the transistors performance. As can be seen in Eq 4.9 the electron mobility μ_n, saturation velocity, v_{sat}, and the channel thickness, b, have a large impact on β. The only parameters left to the disposal of the VLSI designer are the channel width, W, and the channel length L. However, even W and L have physical fabrication limitations which must be adhered to by the VLSI designer. For the Vitesse HGaAs3 process used for this research W could be no larger than 100 um and L could be no smaller then 0.8 um.

For this research many transistors of various sizes were required. The size of a MESFET it best described by its gate length and width. The length of a transistor is the total distance of the gate parallel to the line drawn between the source and drain. The width of a transistor is the size of the gate running parallel to the source and drain. For analog applications larger gate widths are necessary in order to achieve sufficient gain. Gates of sufficient width, say 50 um or greater, necessitate a technique called fingering. As can be seen in Section D of Appendix A, this is a technique to minimize the size of a MESFET and still achieve the necessary gate width to generate the desired gain. For digital applications, minimum size transistors are typically used to minimize power consumption and maximize speed.

The use of GaAs MESFETs have considerably increased the frequency range available to designers. As silicon MOSFETs and BiCMOS technology reach the limit of their lithography capability MESFETs are a logical choice for both analog and digital applications. However, as was mention earlier, GaAs is no panacea and its limitations must be kept in mind when used by the VLSI designer.

3. Project MESFET Performance

For this research, designing of both analog and digital circuits were necessary. Although predominantly an analog thesis, digital circuits will eventually be used in a variety of controlling circuits for the GIC filter. Specific application of MESFETs used in circuits will be discussed in later chapters.

As has been mention, the main purpose for using GaAs MESFETs is their ability to function at much higher frequencies than other available technologies. As was seen in Eq 4.9, β is depends inversely dependent on the gate length and the depth of the depletion layer. The gate length is controlled by fabrication requirements and the depletion layer is dictated by the fabrication process. The depletion layer is reduced by increasing the channel doping. However, this results in an increase in input capacitance. Although these parameters can not typically be controlled by the VLSI designer, it is important for the designer to be aware of the impact of these parameters when planning a design.

The key parameter to evaluate a MESFET is to observe its drain current capabilities under various v_{GS} states. The MESFETs characteristics can best be shown

using a family of curves. Figure 4.11 depicts the general composition of the family of curves for a MESFET. As can be seen, the drain current is nonlinear with respect to the drain-to-source voltage. The family of curves are generated by incrementing v_{GS} starting at V_t. $V_{D,sat}$ is the drain current saturation point for each curve. The effects of this saturation current is a function of the velocity of the electrons not increasing proportionally with the electric field in the channel. This is directly related to the gate length. The gate length plays a critical role in determining the drain current. Decreasing the gate length, results in an increase in the electric field which will cause a lower saturation drain current. If a small $V_{D,sat}$ is desired it is necessary to have a small gate length and visa versa. The short gate length also increases the transconductance and reduces the input capacitance. Section A Appendix B contains the family of curves for the 11 different sized MESFETs which were used in this research. These curves were evaluated using the HSpice circuit simulation software package on a UNIX operating system.

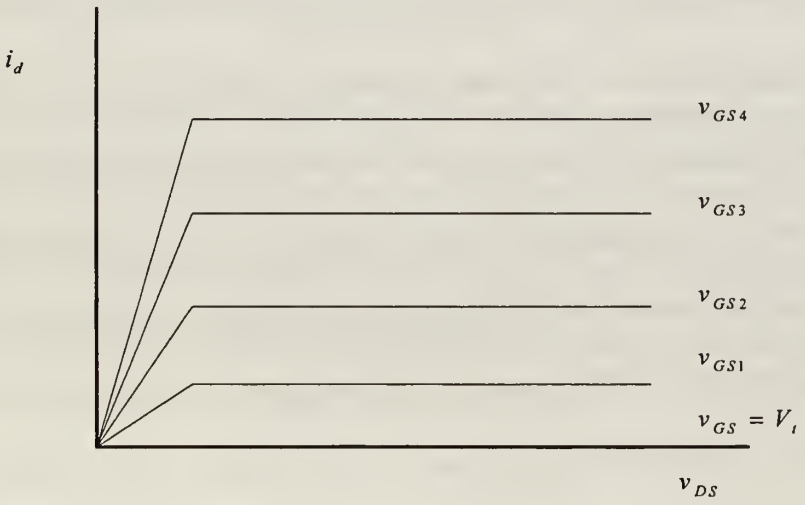


Figure 4.11 MESFET Drain Current vs Drain-to-Source Voltage

D. LOGIC GATES

1. Logic Operation

Digital logic devices are a necessary part of this research. Although the final goal is to implement an analog filter, it is desired that this filter be made programmable. To enable this programming it is necessary to implement basic logic devices that will be used. The basic purpose of logic devices is to take inputs and given a specific evaluation process, provide an output of either true or false. Electronically true is usually, but not always, represented by a "high" voltage or **1** and false is represented by a "low" voltage or **0**. The whole class of mathematics, Boolean Algebra is dedicated to conducting mathematical operations using just **1's** and **0**'s. It is not the intent here to provide an extensive discussion on Boolean Algebra but it is necessary to provide some of the basics for a complete understanding of this research.

As can be seen in Table 4.4 there are seven different gates that are typically used. Also shown is the Boolean Algebra expression and truth table for that gate. While the gates show only two inputs gates using more than two are routinely used. The variables or formulas with the line over them are referred to as "bar" (e.g. $\overline{A} = A''bar''$). This is also commonly referred to as A-not or not-A. The NOT gate is also known as an inverter, since its output is the opposite of its input: If the input is a **1,** then the corresponding output is a **0** and vice versa. The AND gate has the property that its output is a **1** if both of its inputs are **1**s. The NAND operation is the negation of the AND operation. The OR gate output is a **1** if either of its inputs are a **1**. The NOR gate is the negation of the OR

gate. The XOR, exclusive-OR, gate output is a **1** if an odd number of inputs is a **1**. And finally, the XNOR gate is the negation of the NOR gate.

Logic Gate	Input A	Input B	Output	Symbol
NOT	0	na	1	
AND	0 0 1 1	0 1 0 1	0 0 0 1	
NAND	0 0 1 1	0 1 0 1	1 1 1 0	
OR	0 0 1 1	0 1 0 1	0 1 1 1	
NOR	0 0 1 1	0 1 0 1	1 0 0 0	
XOR	0 0 1 1	0 1 0 1	0 1 1 0	
XNOR	0 0 1 1	0 1 0 1	1 0 0 1	

Table 4.4 Logic Gates

Unlike the silicon MOS logic, GaAs does not have a standard method of logic circuit implementation. This situation can be explained for two reasons. Lacking a complementary device there are multiple ways to achieve a logic output using GaAs, each having its own advantages and disadvantages. Second, GaAs is relatively new and is maturing.

Direct-coupled FET logic (DCFL) is by far the most widely used and simplest form of GaAs logic circuits. In this form of logic both depletion MESFETs and

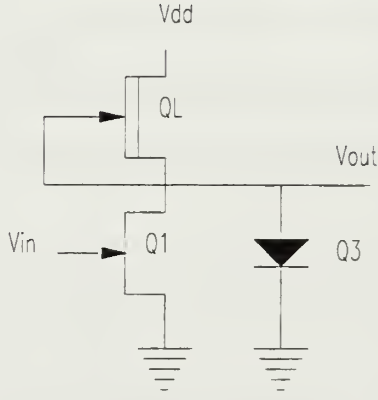


Figure 4.12 DCFL Inverter, Sedra (1991)

enhancement MESFETs are used. Figure 4.12 shows the a DCFL inverter configuration. Q_L is a depletion MESFET, were V_{DD} is typically tied to 2V and is referred to as the load transistor. The purpose of this transistor is to provide the voltage for the high output or **1**. Q1 is an enhanced MESFET whose source is tied to ground, drain tied to the source of QL and whose gate provides the input to the inverter. The purpose of Q1 is to provide the voltage level for an output low or **0**. Q3 is a SBD which is used to clamp the voltage level of the output high, V_{OL} condition. As can be seen in Figure 4.12, as long as v_i is less than V_{TQ1}, v_o voltage will be set by Q3 (i.e. .7V). As v_i increases to some value $\geq V_{TQ1}$ Q3 ceases to conduct and v_o will be set by the voltage at the source of Q_1 thus achieving an output low, V_{OL}. V_{OL} will actually reach a value slightly higher than Q1 which is equal to the voltage drop across the transistor Q1. The slope of the line from the output high to the output low state is determined largely in part by the characteristics of

Q1 operating in the triode region. Figure 4.13 depicts a notional performance of an inverter. A diode-configured-MESFET is typically used for the SBD as was mentioned earlier. The VLSI layout of the inverter constructed for this research can be seen in Section E Appendix A.

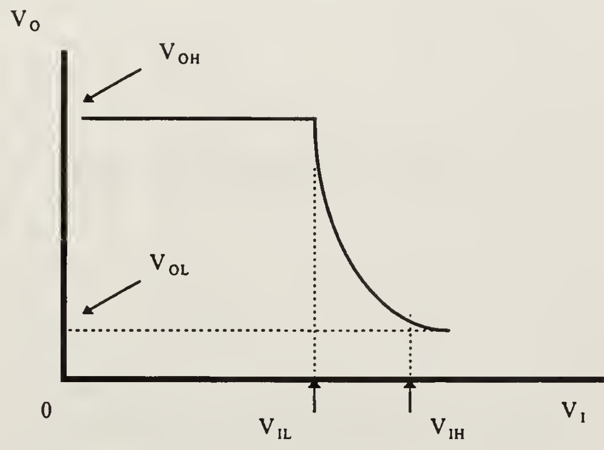


Figure 4.13 Transfer Characteristics of a DCFL Inverter

The next primary gate which is used in GaAs DCFL circuits is the NOR gate. The advantage of using the NOR gate is two fold. First, by using the NOR gate the logic designer can realize any other logic gate. For example; to create an inverter from a NOR gate it is only necessary to take the input and apply it to both inputs of the NOR gate. For another example, to create an AND gate from a NOR gate it is a simple matter of inverting the two inputs and then apply the outputs of the inverters to the inputs of the NOR gate. The second advantage of the GaAs DCFL NOR gate is the ease at which it is constructed. As can be seen in Figure 4.14 the NOR can be seen as a modification of the NOT gate. It is only necessary to add an additional enhancement MESFET for each

additional input to the NOR gate. Using the inverter and the NOR gate it is possible to realize all necessary logic the designer would need.

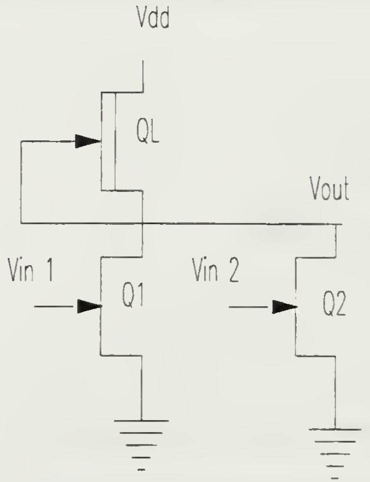


Figure 4.14 DCFL NOR Gate, Sedra (1991)

2. Project Logic Construction

The designs mentioned above are those used in this research. Eventually this logic will be used to select the various types of filters available and the Q factor of the filter. The other application for the logic is in switched capacitor networks which will be discussed in the next chapter. The VLSI implementation of the NOT gate can be seen in section E of Appendix A. The VLSI implementation of the NOR gate can be seen in section F of Appendix A. Figure 4.15 depicts the schematic description of the NOT gate constructed and the gate sizes used. Figure 4.16 depicts the schematic description of the NOR gate constructed.

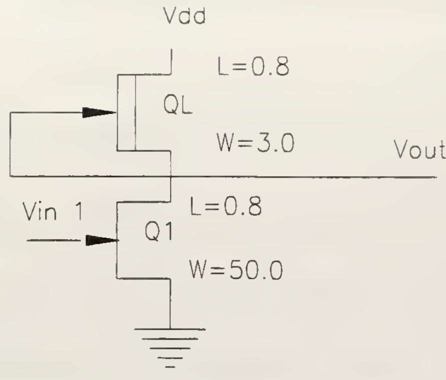


Figure 4.15 Project DCFL Inverter

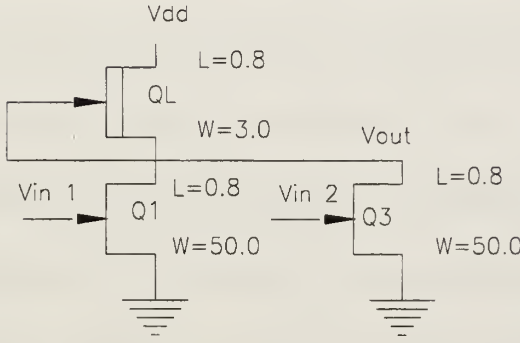


Figure 4.16 Project DCFL NOR Gate

In this chapter a variety of GaAs components have been presented. All of these components contribute directly to the completion of this project. It is in the best interest of the designer to fully understand the capabilities and limitations of these components in order to best employ them. One such use of the capacitor and MESFET is the construction of switched capacitor circuits. Switched capacitor circuits are an efficient method of representing a resistance in a VLSI system. It is this subject which is discussed in the next chapter.

V. SWITCHED CAPACITOR NETWORKS

A. THE NEED FOR SWITCHED CAPACITORS

As was mention in Chapter II, the construction of the GIC filter requires capacitors and admittance values. Again recall that an admittance is the inverse of a resistance. The implementation of capacitors in VLSI can be accomplished with very exacting accuracy. However, resistance values are extremely difficult to construct to exacting values and can vary as much as 50 % on the same chip. Another drawback of resistors in VLSI is the fact that they require a large chip area to achieve the necessary resistance and hence become physically prohibitive. To over come this situation, a switched capacitor network may be constructed to emulate the required resistance. Capacitors are VLSI friendly for two reasons. First they can be implemented to very exacting values and with a tolerance of 0.1% of each other. Second, they require much less area on an IC chip than a resistor.

B. SWITCHED CAPACITOR OPERATION

The design of such a system is fairly easy and an ideal solution for constructing resistors in VLSI applications. A switched capacitor is in a sense a capacitor connected to switches which turn on and off. More specifically, if a capacitor C_1 is connected to a voltage source V_1 then the capacitor stores an amount of charge $Q_1 = C_1V_1$.

If we then connect the capacitor to node V_2 the capacitor is then recharged to $Q_2 = C_1V_2$. The amount of charge transferred from V_1 to V_2 can be seen in Eq 5.1. Now if

$$\Delta Q = C(V_1 - V_2) \qquad \text{(Eq 5.1)}$$

this process is repeated continually so that the switching occurs at a rate much greater than the frequency of the signal from V_1 and V_2 then it can be assumed that the two signals are constant over the period T. The amount of charge flowing can be considered a current as described in Eq 5.2. This then indicates that a switched capacitor functions as a resistor as can be seen in Eq 5.3.

$$I = f_c C_1 (V_1 - V_2) \qquad \text{(Eq 5.2)}$$

$$R = \frac{V_1 - V_2}{I} = \frac{1}{f_c C_1} \qquad \text{(Eq 5.3)}$$

Recall from Chapter II and as seen in Eq 5.4 that the center frequency of a filter is set by the inverse of a RC product. Therefore, from Eq5.3 and 5.4 ω_0 can be expressed as a ratio of capacitors according to eq 5.5.

$$\omega_0 = \frac{1}{RC} \qquad \text{(Eq 5.4)}$$

$$\omega_0 = \frac{C_1}{f_c C} \qquad \text{(Eq 5.5)}$$

A graphical depiction of this procedure is shown in Figure 5.1. The ability

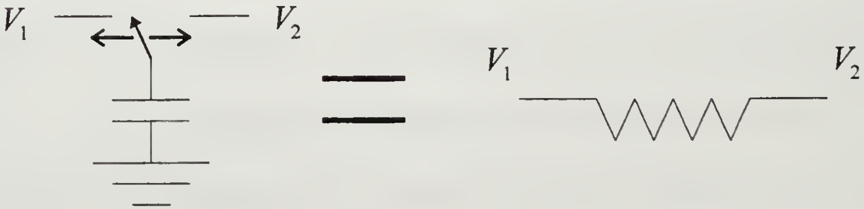


Figure 5.1 Simple Switched Capacitor System

to create a resistor in VLSI may be accomplished by the construction a capacitor of a fixed value and clocking it at a rate to achieve the desired resistance. For example; a 1pf capacitor clocked at 100kHz achieves a resistance equivalence of 10M ohms.

At this point, it must be stressed that the clocked frequency of the switched capacitor must be much greater than the input signal frequency. A rule of thumb is to have the clock rate of at least 10 times that of the signal, which is more than enough to satisfy the Nyquist criteria. The Nyquist rate addresses the rate at which a signal needs to be sampled in order to distinguish it from another signal or for a successful recovery. The Nyquist rate of a signal is a rate at least twice the highest frequency component of a given signal. The switched capacitor clock rate is the rate required to charge and discharge a capacitor in order to ensure an adequate amount energy of the incoming signal is present to extract the signal from the output of the capacitor.

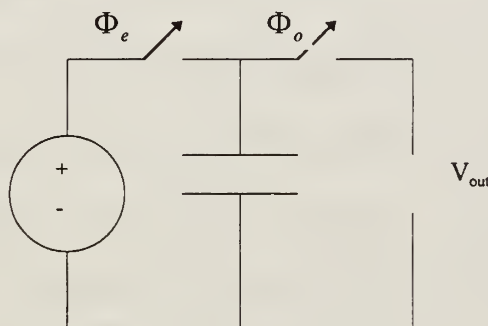


Figure 5.2 Switched Capacitor Network, Allen (1984)

Figure 5.2 depicts a more exact representation of an actual network. In this figure both switches are shown in the open position. In fact both switches would be out of phase in order to permit the charging of the capacitor when one switched is closed and

discharging upon the opening of the first switched and the closure of the second switched. This non-overlapping is required to prevent the short circuit from V_1 to V_2 which would occur if both switches were closed simultaneously. It is possible to clock a switched capacitor network with more than two phases for more demanding signals. In this research the switched network was limited to a two phase clock scheme. Switched capacitor networks which use a two phase clock is commonly referred to as a bi-phase network. Figure 5.3 demonstrates the timing relationships necessary in a bi-phase network. As can be seen in this figure, there is no point in time when both Φ_o and Φ_e are high at the same time. This figure is assuming that the higher voltage is the voltage necessary to "turn on" the switched.

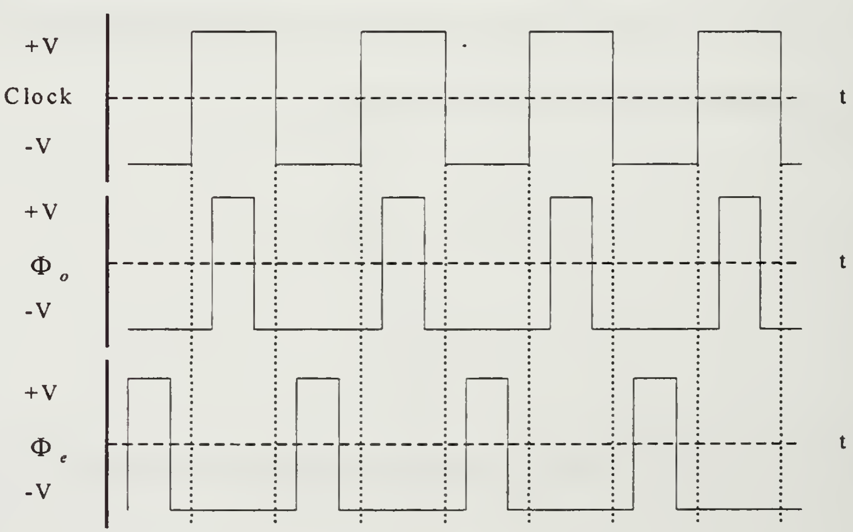


Figure 5.3 Two Phase Non-overlapping Clock

C. BI-PHASE SWITCHED CAPACITOR NETWORKS

The biphase switched capacitor network is best viewed as two totally separate systems. When the even phase is active, one system is active and when the odd phase is

active, the other system is active. The output of the even system after one cycle is used to determine the initial condition for the input of the odd system at the next cycle and then the odd output is then used as the initial condition for the even input and so on. The aggregate of the sampled wave forms from the two systems result in the output of the entire system. This approach of switched capacitor networks is best accomplished using CAD design tools. The other method for building and designing switched capacitor network is to combine the even and odd systems into a single system and use z-transforms to analyze the system in the z-domain.

D. THE BI-LINEAR RESISTOR

One configuration used to maximize the efficiency of the switched capacitor network is the bilinear resistor. There are four basic switched capacitor networks used to achieve resistance equivalence. First, as seen in Figure 5.4, there is the parallel switched capacitor resistor realization whose resistance equivalence is shown in Eq 5.6. Second, as seen in Figure 5.5, there is the series switched capacitor whose resistance equivalence is shown in Eq 5.6. Third, as seen in Figure 5.6, there is the series parallel switched capacitor whose resistance equivalence is shown in Eq 5.7. Finally, as seen in Figure 5.7 , there is the bilinear switched capacitor network whose resistance equivalence can be seen in Eq 5.8.

$$R = \frac{1}{f_c C} \qquad \text{(Eq 5.6)}$$

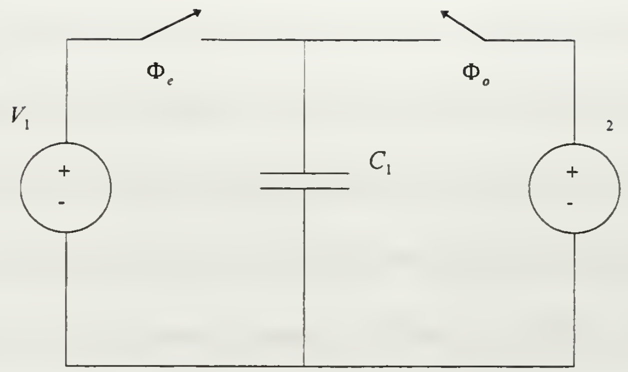


Figure 5.4 Parallel Switched Capacitor Network, Allen (1984)

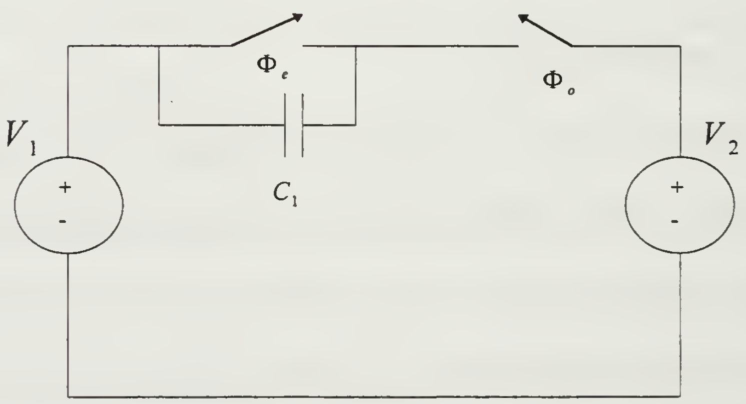


Figure 5.5 Series Switched Capacitor Network, Allen (1984)

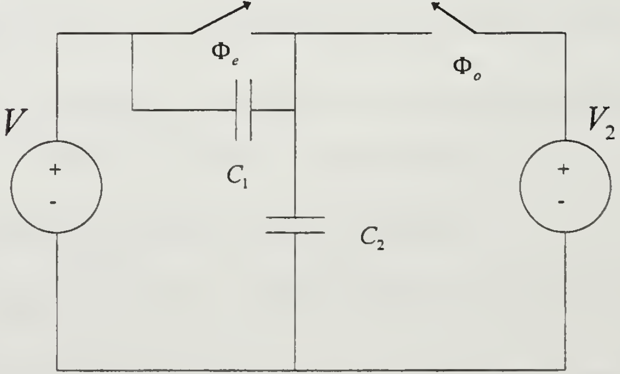


Figure 5.6 Series-Parallel Switched Capacitor Network, Allen (1984)

$$R = \frac{1}{2f_c C_{tot}} = \frac{1}{2f_c(C_1 + C_2)} \qquad \text{(Eq 5.7)}$$

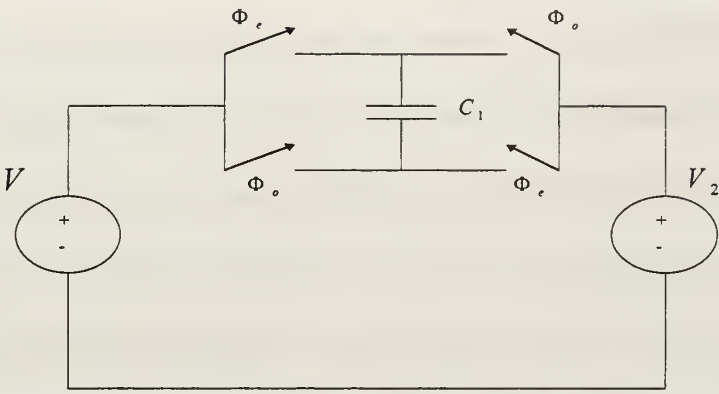


Figure 5.7 Bilinear Switched Capacitor Network, Allen (1984)

Recall again from Chapter II that the GIC filter was evaluated by determining its admittance values. Also, recall that the admittance is the inverse of the resistance. Therefore it is possible to determine the appropriate clock frequency and the capacitor value to obtain the desired equivalent admittance using Eq 5.8 when using the bilinear switched capacitor network. The derivation of Eq 5.8 is covered in Schaumann (1990).

$$R = \frac{1}{4f_c C} \qquad \text{(Eq 5.8)}$$

E. PROJECT TWO PHASE CLOCK

As was mentioned above an integral part of the switched capacitor network is the two phase clock. The purpose of the clock is to provide the switching signal necessary to

drive the switched network. There are three important characteristics a clock must possess in order to be effective in switched networks. First, the clock must be able to operate at extremely high frequencies. Recall that the capacitor must be charged and discharged at a rate of at least 10X that of the highest frequency ofthe input signal. Second, the clock must provide adequate time in its period to permit the switches (MESFETs) to turn on and off. The driving factor for this is the characteristics of the MESFETs, but the clock is designed with this limitation in mind. Third, the output voltages of the clock must be adequate to trigger the switches being used in the switched capacitor network.

There are many methods which can be used to realize a two phase clock. The most common method is by employing the use of a single clock and logic the provide the two phase split. As can be seen in Figure 5.8, a two phase clock is made up of a clock

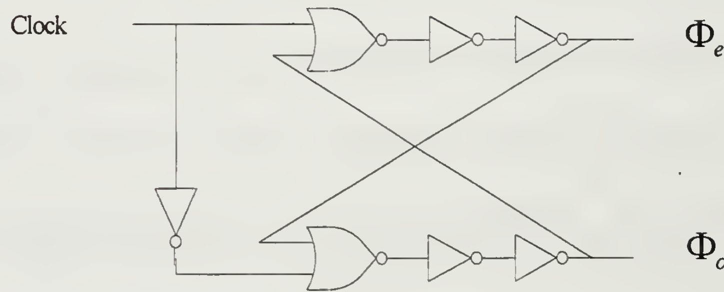


Figure 5.8 Two Phase Non-overlapping Clock, Schaumann (1990)

input, two NOR gates and an odd number of NOT gates. The purpose of the NOR gates is to alternate the clock pulse. The purpose of the first NOT gate is to induce a 180 phase shift in one side of the clock such that it is 180 degrees out of phase with respect to the other side. The purpose of the remaining NOT gates is to provide adequate de;ay to ensure nonoverlapping. As the number of inverters is increased, the width of the pulse

narrows. The number of pulse shaping inverters necessary will be determined by a couple of factors. The first factor is determined by the switching speed capability of the MESFETs being used as the switches in the switched capacitor network. However, it is unlikely that this will be the limiting factor. Assuming that it is desired to maximize the clock capability, the limiting factor will most likely be the characteristics of the logic gates used. The number of pulse shaping NOT gates will therefore be equal to number that can be placed in the circuit and still provide adequate rise time and hold time to the nth NOT gate. At the point where a NOT gate is added forcing the output pulse width to contain less time than the rise time and hold time required for the input of the clock, the clock will cease to function. This evaluation approach fixes the input clock frequency to some maximum rate. The maximum input clock frequency may be determined by either equipment capabilities or circuit requirements as determined by the signal processed by the switched capacitor network. Another design consideration is that the feed back from the output of the nth NOT gate must be from an odd number of gates in order to provide the proper input into the NOR gates to continue the clock in a proper fashion.

Using the logic gates as described in Chapter IV, the two phase non overlapping clock for this project was constructed as shown in Figure 5.8. Voltage input for this clock will be from 0.0V to 0.7V. These voltages were chosen because these are typically used as DCFL input voltages. The resulting output from the clock is 0.05V to 0.7V. The output using these parameters and a 1GHz clock can be seen in Section B of Appendix B. The VLSI implementation of this circuit can be seen in Section G of Appendix A.

As will be described in the next section the output from the clock described above is inadequate to properly drive the switched capacitor circuit. To properly adapt the clock output, it was necessary to design a voltage shifter/amplifier circuit which would provide the necessary voltage levels to drive the switched capacitor circuit. This component is described below.

F. PROJECT CLOCK AMPLIFICATION

As was mentioned above the output of the clock provides a voltage swing from 0.05V to 0.7V thus providing a 0.65 voltage swing. In this research it was decided to use the depletion MESFET in the switched capacitor network for the simple reason that they are inherently faster than their enhancement MESFET sibling. It should be recalled that it is necessary to use negative voltages to "turn on" a depletion MESFET. The MESFET used in the switched capacitor network will therefore have a V_t of -0.7V. To ensure that the MESFET is completely saturated and completely turned off, it is also necessary to not only shift the voltage level but also increase the voltage swing from 0.65V to 1.5V and center this swing around -0.7V. To accomplish this a clock amplifier was constructed.

There are two approaches to this problem. The signal could first be shifted then amplified or it could be amplified then shifted. The amplification then shift method was chosen for this project. Figure 5.9 depicts the schematic of the circuit used in this research. This circuit was capable of a voltage swing from -1.6V to -.08V. The output of this circuit can be seen in Section C Appendix B. The VLSI implementation of this circuit can be seen in Section H Appendix A.

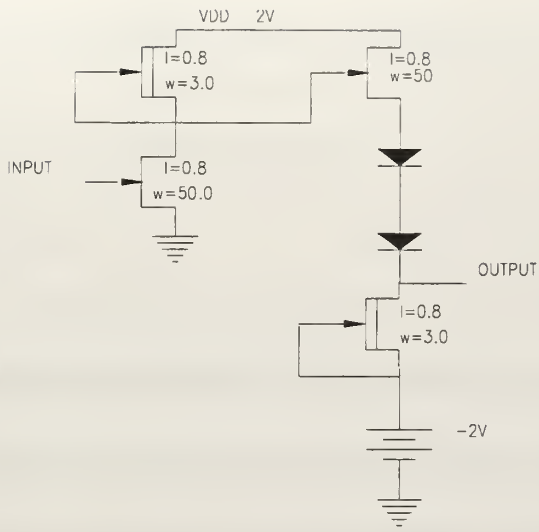


Figure 5.9 Clock Amplifier/Shifter

G. PROJECT SWITCHED CAPACITOR NETWORK

The switched capacitor network constructed for this research is a combination of the components previously described. The bilinear switched capacitor resistor network was used in this research. To construct this device, minimum size depletion MESFETs were used in conjunction with the 0.5pF capacitor described in Chapter IV. Figure 5.10 depicts the schematic of the bilinear switched capacitor resistor network, where Φ_e and Φ_o are the two distinct phases coming from the two phase non-overlapping clock. The output of this network can be seen in Section D Appendix B. Using an input signal of 1 MHz, the switched capacitor network was clocked in order to view the effective output. Using a 10 MHz clock the input signal is discernible when only viewing one cycle of the output sine wave. When the clock frequency is increased to 100 MHZ, the clarity of the input signal was exceptional. The VLSI layout of the switched capacitor network constructed for this research can be seen in Section I Appendix A.

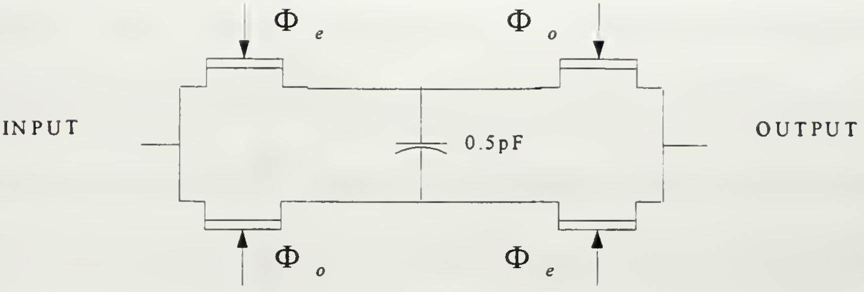


Figure 5.10 Bilinear Switched Capacitor Network

In this chapter, a means to overcome the inability of VLSI to achieve accurate resistors was discussed. By employing switched capacitors the VLSI designer has direct control over the resistance that is implemented. This resistance provides an integral part to the development of the GIC filter. The other major component that makes up the GIC filter is the operational amplifier. The operational amplifier is the heart of the active filter and is discussed in the next chapter.

VI. OPERATIONAL AMPLIFIERS

A. OPERATIONAL AMPLIFIER BACKGROUND

1. Introduction

The operational amplifier plays a major role in electronics in all areas from communications to audio reproduction. As was mentioned in Chapter II the operational amplifier (OPAMP) is the cornerstone of active filters of all types. This, of course, is true for the GIC filter as well. To fully understand how the OPAMP functions within the GIC filter it is necessary to have an understanding of how it is constructed.

2. OPAMP Basics

The OPAMP is typically designed with three stages. The first stage is a high-input impedance differential amplifier. The second is a high gain stage. The third stage is a low-impedance output stage. OPAMPs typically have two differential inputs and one output. Figure 6.1 depicts the symbol for an OPAMP.

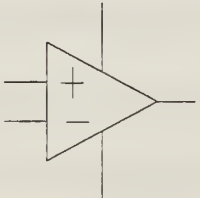


Figure 6.1 OPAMP Symbol

To best understand real OPAMPs it is helpful to study ideal OPAMP characteristics which real OPAMPs closely resemble. An ideal OPAMP can be defined as a device that has a differential input, single output amplifier with infinite gain, infinite

input resistance, and zero output resistance. Figure 6.2 depicts a schematic of the ideal case OPAMP. As can be seen in Figure 6.2 the OPAMP responds only to the difference between the two inputs. This difference is then multiplied by factor A. The factor A is the open loop gain of the OPAMP itself. Although OPAMPs can come close to achieving ideal conditions, there are non-ideal characteristics which are used as parameters for evaluating OPAMP performance.

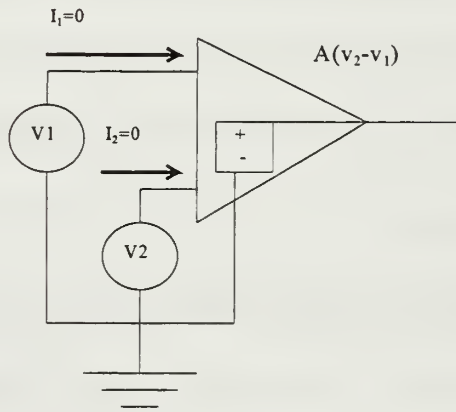


Figure 6.2 Equivalent Circuit for Ideal OPAMP, Sedra (1991)

Ideally the input impedance of an OPAMP should be infinite. The input impedance of a OPAMP is defined as the ratio of the input voltage to input current. Input impedance should be as large as possible in order to have better performance. However, infinite impedance is not possible and typical OPAMPs will have an input impedance ranging between 100k Ohms to 10M Ohms.

The ideal output impedance should be zero. The output impedance is defined as the ratio of the open-circuit output voltage to short circuit output current of an OPAMP. Just as it is not possible to have infinite input impedance it is also not possible to have

zero output impedance. Typical output impedance values of commercial OPAMPs range from 2 ohms to 2k ohms. These values are low enough in most cases that permit the designer to assume that it is actually zero which will allow the OPAMP to be considered as an ideal voltage source.

Since the input impedance is not infinite there will in fact be current flowing into the inputs of the OPAMP. This current is referred to as the input bias current. Real OPAMPS will have input bias currents ranging from 10^{-9} to 10^{-12} amps. Commercial OPAMPs will be designed with a stated average value for the input bias current, I_B. Eq 6.1 shows the method to determine the input bias current. As can be seen in this equation both input currents are assumed to be of equal value. Again this is not the case and in order to achieve this conditions the designer of OPAMPs will specify an input offset current, I_{os}. Eq 6.2 depicts the method by which I_{os} is determined. Additionally, as seen in Figure 6.2, when the input voltages are equal, the output should be zero. However, due to the imperfection of the balance in the different stages, a slight bias voltage to one of the inputs is needed. This input offset voltage will then correct the output voltage to be zero.

$$I_B = \frac{I_{B1} + I_{B2}}{2} \qquad \text{(Eq 6.1)}$$

$$I_{os} = \left| I_{B1} - I_{B2} \right| \qquad \text{(Eq 6.2)}$$

The three primary parameters that are typically evaluated and used for OPAMP performance comparison are; Common Mode Rejection Ratio (CMRR), Slew Rate (SR),

Frequency Response, and Gain-Bandwidth Product (GBWP). These parameters provide the designer with the key information necessary to effectively employ OPAMPs.

CMRR can be defined as the ability of a device to amplify differential signals while rejecting common-mode signals. An ideal OPAMP would ignore all signals common to both of the inputs. This is to say that if two identical signals are applied to the inputs the output of the OPAMP should be zero. Real OPAMPs are not capable of performing a perfect differential function, and therefore some common signals are permitted to pass. Eq 6.3 shows the mathematical expression used to calculate the CMRR. Since this equation is a unit-less ratio and normally very high, CMRR is usually expressed in dB.

$$CMRR = \frac{|A|}{|A_{cm}|} \qquad \text{(Eq 6.3)}$$

The second parameter of great interest is the Slew Rate (SR). SR is defined as the maximum amount of change in output voltage over a specific period of time. The cause for variation is due to internal capacitance within the OPAMP. The capacitance creates a situation where the output will lag behind the input. The general trend is that at higher frequencies and high signal levels there are higher rates of signal change. Eq 6.4 depicts the mathematical expression for SR.

$$SR = \frac{\Delta V_{out(\max)}}{\Delta t} \qquad \text{(Eq 6.4)}$$

The frequency response is defined as the frequency at which the OPAMP gain fall to the 3db point below its maximum gain (Half power point).This is due to existence of

the pole produced by the internal compensating capacitor. This characteristic therefore provides a limitation to the bandwidth which an OPAMP can effectively function. Figure 6.3 demonstrates the method by which the open loop gain of an OPAMP is determined, where f_b is the break frequency and f_t is the unity-gain frequency.

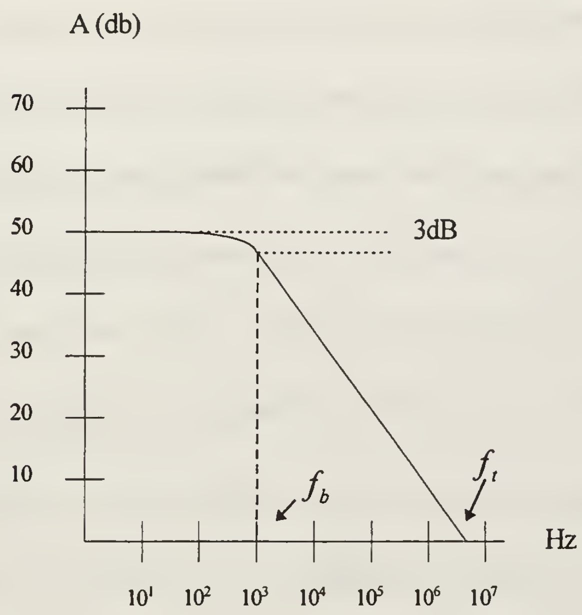


Figure 6.3 Frequency Response of an OPAMP

The last major parameter of an OPAMP is the GBWP. This is defined as gain of an OPAMP times its bandwidth which is also equal to the unity-gain frequency. Eq 6.6 shows the GBWP calculation.

$$\text{GBWP} = \text{unity-gain frequency x unity gain} \qquad \text{(Eq 6.5)}$$

B. PROJECT AMPLIFIER CONSTRUCTION

The OPAMP used in this research was one developed in previous research in Carson (1995). This OPAMP was designed specifically to be used as apart of more

complex composite OPAMP designs and switched capacitor networks. Since this design has yet to be fabricated as either a composite OPAMP or stand alone OPAMP, the intent of this research was to conduct additional testing and prepare the design for fabrication. It is not the intent to reiterate the research accomplished earlier. However, it is necessary to present and describe the design. Figure 6.4 shows the final design of the final OPAMP. This differential OPAMP used depletion MESFETs exclusively. All MESFETs gate lengths are 0.8 um. The gate widths of each MESFET are shown in parenthesis. The large gate widths were used to overcome the low intrinsic gain produced by GaAs MESFETs. SBDs were used to accomplish level shifting. A SBD configured MESFET, as was discussed in Chapter IV, was employed to accomplish this task.

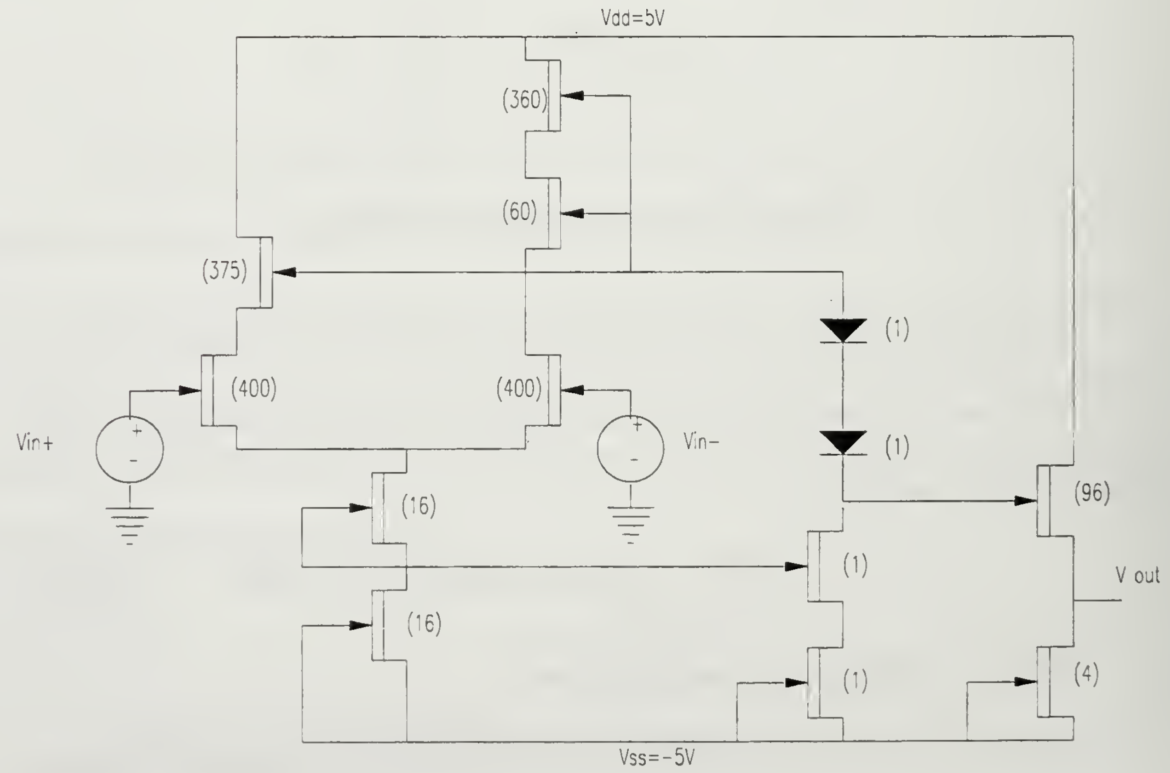


Figure 6.4 Project GaAs OPAMP, Carson (1995)

C. PROJECT AMPLIFIER PERFORMANCE

In order to effectively conduct this research and prepare for the construction of the filter components it was necessary to conduct the analysis done in Carson (1995). It is not the intent at this point to reiterate the entirety of Carson (1995) but it is necessary to present the final analysis conducted by this author for followon research. The evaluation conducted was nearly identical to that conducted in Carson (1995). Standard testing procedures using the HSpice simulation software were conducted and are discussed below.

1. Offset Voltage

As was mentioned earlier in this chapter, the offset voltage is the voltage necessary to one input such that there is no differential between v+ input and v- input. Therefore, the offset voltage, V_{os}, must be equal in magnitude and opposite to the voltage that was applied to reach zero gain. Figure 6.5 depicts the OPAMP configuration necessary to evaluate V_{os}. V_{os} was found to be 47.93uV. The HSpice simulations of this effect can be seen in Section E Appendix B.

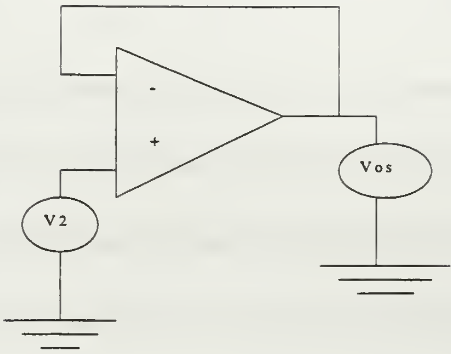


Figure 6.5 Offset Voltage Test

2. Open-Loop Gain and Phase

As was mentioned above, the open-loop gain of an OPAMP will indicate what is the maximum amount of gain one can expect to get from the OPAMP. The OPAMP performed remarkably well achieving 22.7 dB of gain out to 25 MHz. Using the data in Section E Appendix B and Eq 6.5, a GBWP of 4.5 GHz was achieved. It is the GBWP of GaAs OPAMPs that make them an ideal choice for high frequency operations. It should be mentioned that this is not a terribly high gain for an OPAMP, especially silicon OPAMPs, however silicon would be incapable of operating at this frequency.

3. Common Mode Rejection Ratio (CMRR)

The CMRR was evaluated by determining the common mode gain and the use of Eq 6.3. The common mode data can be seen in Section E Appendix B. With this data, the CMRR was found to be 32 dB.

4. Slew Rate (SR)

As was mentioned earlier, the slew rate is the rate of change of the output voltage in response to fst changing input. To conduct this evaluation a 1 GHz pulse of width of 50 ns was sent through the OPAMP. The SR was then measured as the slope of the line from the maximum to minimum voltage applied. Using Eq 6.4 and data from the simulation, found in Section E Appendix B, a SR of 1747 V/us was determined.

The OPAMP designed in Carson (1995) appears to be well suited for use in this research. As was discussed in Carson (1995), if additional gain is necessary this OPAMP can be configured in a composite design to provide this capability. The VLSI layout of this OPAMP can be seen in Section J Appendix A.

Now with all the necessary components needed for the construction of a GIC switched capacitor filter discussed, it is now necessary to discuss how the chip construction was accomplished.

VII. PROJECT VLSI LAYOUT

A. INTRODUCTION

The process of taking an idea of a VLSI circuit and having it fabricated requires substantial research and detailed preparations. The majority of the research conducted was spent researching means, methods and procedures necessary to have a GaAs VLSI chip fabricated. The purpose of this chapter is provide a description of the planning and procedures conducted in order to complete this research.

B. MOSIS

The MOSIS service is a low-cost means for the fabrication of custom designed VLSI chips. The purpose of MOSIS is to provide government and university research labs with a venue to fabricate their VLSI designs. This is achieved by compiling all VLSI requests for a wafer which is then processed by established chip manufacturing firms. This allows VLSI designers and researchers to acquire small quantities and share wafer fabrication cost for a substantial savings. Depending on the technology chosen, the number of parts available can be as few as four and as many as 25. The technologies available through the MOSIS service are shown in Table 7.1. Each week there is a run of one of the technologies listed. Depending on the general demand of a technology some have one run a month (0.8 HP) while other less popular processes have no more than two to four runs a year (0.8 GaAs). Submission deadlines for designs are published nine months to one year ahead of the scheduled fabrication run.

Size um	Process	Manufacturer
2.0	CMOS	Orbit
1.2	CMOS	Orbit
1.2	CMOS	HP
0.8	CMOS	HP
0.5	CMOS	HP
0.8	GaAs	Vitesse

Table 7.1 MOSIS Available Technologies

Designs are submitted to MOSIS either through the Internet or through physical means. Designs must be submitted in either a CIF format or a UU-encoded GDSII or MEBES format. All designs must pass the design rule check (DRC) for the appropriate technology. Upon receipt of a design file MOSIS will run a DRC. If the design does not pass the DRC it will be rejected and returned to the originator. It is recommended that designers make reservations for their run of interest in order to ensure room on the wafer. All arrangements for fabrication and design submissions at the Naval Postgraduate School must be submitted through the MOSIS representative.

C. VLSI TOOLS

There exist numerous CAD tools which are capable of properly producing VLSI layouts which are acceptable by MOSIS. Table 7.2 shows those CAD tools which are noted by MOSIS as compatible with the MOSIS service. Of these CAD tools, three of them will be discussed in detail below.

CAD Tool	Capability
Cadence	SCMOS, CMOSN, CMOSX
Cascade	HP CMOS34, HP CMOS26, Vitesse HGaAs3
Mentor Graphics	SCMOS, CMOSN
Magic	CMOSN, Vitesse HGaAs3
Synopsys	CMOSN, CMOSX
Tanner Research	SCMOS

Table 7.2 MOSIS Supported CAD Tools

An important aspect of all CAD tools are technology files. A technology file is a file containing the necessary information of a specific technology for a specific CAD tool. The information in the technology file provides information on design rules which must be satisfied for the specific fabrication process it was written for. Minimum gate length, minimum via size between layers, minimum distance from gate to source and minimum routing metal width are examples of just some of the design requirements that are contained in a technology file. It is very important that a new VLSI designer become familiar with the technology file for the CAD tool to be used. A tremendous amount of time for this project was spent researching technology files, their availability and capability. Without the appropriate CAD tool and technology file combination, the designer will be unable to realize his design as desired. Of the listed CAD tools only the Cadence and Magic CAD tool packages were available for this research. However, as can be seen, only the Magic CAD tool has the ability to process GaAs designs. More on these tools will be discussed below.

Obtaining information about MOSIS services and capabilities improved tremendously over the course of this research. Initially only the FTP site at FTP.MOSIS.EDU was available. MOSIS then established a web site at http://www.isi.edu/mosis. The web site provides information about fabrication schedules, data from previous MOSIS fabrication runs, packaging information and pricing.

1. Cadence

Initial VLSI layout experience was gained by using the Cadence CAD tool. Layout functions in Cadence are accomplished in the Virtuoso layout package. Virtuoso is an IC layout, processing and analysis package capable of custom designs, automatic component generation, layout compaction, layout synthesis, layout-schematic validation and layout Spice file generation. Although initially there existed configuration difficulties, Virtuoso proved to be an extremely capable CAD package.

There are certain capabilities contained in the Virtuoso package that are worthy of mention. Virtuoso provides the cability for the designer to produce individual components in layout form, and then associate that layout with a designer generated symbol. Layout procedures are continuously monitored by Virtuoso and immediately notifies the designer of any design rule violation. Once the layout and symbol have been generated and named, Virtuoso provides the ability to conducted a layout versus schematic (LVS) reconciliation process between the two. The designer is then able to construct VLSI circuits in a schematic form using the designer generated symbols. Should certain parameters within a layout need modification (i.e., gate length) it is not necessary to construct an entirely new layout but only to change those parameters within

the layout cell information. Once the design is completed Virtuoso has the ability to automatically generate a Spice file which they can run on the Cadence supplied USpectre circuit analysis package or any other user supplied Spice analysis package. Both analog and digital simulations are available in the Virtuoso package. Finally, should a designer decide to embark on a large design effort, there exist commercially available libraries containing simple gates to arithmetic logic units.

The above description of the capabilities of the Virtuoso VLSI CAD package is provided to give insight into where VLSI design is today.

2. Compass

The COMPASS design CAD tool is very similar to the Cadence CAD tool. No research was conducted using this CAD tool however, the author did have the opportunity to view this CAD tool at the 1996 IEEE GaAs IC Symposium. The COMPASS tool possessed all the capabilities mentioned above. The COMPASS CAD tool is mentioned only because it is the only "modern" CAD tool that is widely used for GaAs IC fabrication.

3. Magic

The final CAD tool to be discussed is the one used for this research. Magic is primitive as compared to the above mentioned CAD tools. First developed in the mid-1970's Magic is truly the grandfather of VLSI CAD tools. As the only GaAs capable CAD tool available for this research, Magic was the mainstay for this project. Unlike Cadence and COMPASS, all VLSI layouts must be individually constructed. Magic does provide the ability for the continuous monitoring of design rules. If a design rule is

violated, the designer is automatically notified. Great care must be taken by the designer when using Magic to ensure proper VLSI layout. Unlike Cadence, a schematic is not generated and therefore a LVS check is not needed. Also, Magic does not possess the ability to generate Spice files for subsequent analysis. Analysis for GaAs circuits using the Vitesse fabrication process must use the HSpice analysis package. Since there is not a LVS process, Magic is also not capable of producing self generated Spice files. Unlike Cadence which would detect layout-circuit errors, Magic provides no ability to discover and correct layout-circuit errors. The benefit of the Magic CAD tool is that since it has been in use for such a long time, all of the problems have been corrected. All layouts presented in Appendix A were constructed in Magic.

D. VLSI IC CHIP PADS

Before discussing the project chip construction there is a need to discuss the interface that is beneficial for an effective chip. After completing the design and layout of the components necessary for the construction of the GIC filter, additional components were necessary to provide protection and capability for the circuits that are to be placed on the chip. Pad is the term used to describe the point on the chip where power and input/output interfaces are placed. The pads are connected to the circuits on the interior of the chip and to the pins on the chip package. The minimum size pad area for the MOSIS packaging process is 100um per side.

1. Power Pad

The power pad is used to provide pad Vdd and pad Vss to the chip. This power should not be confused with the circuit Vdd and circuit Vss which is run separately from pad power. No significant design is necessary to implement the power pad. Typically there are multiple power pads on the same chip. The reason for multiple power pads is to prevent starving those circuits on the opposite side of the chip of the power pads. Power pads are connected to continuous bands of metal that surround the perimeter of the chip. For this project two pads were used for Vdd and were connected to metal 1 and 2 pads were used for Vss and connected to metal two.

2. Driver Pad

Driver pads are used with digital circuits to provide both electrostatic discharge protection and to improve current drive capability. The driver pads used for this project were obtained from Professor Douglas Fouts of the Naval Postgraduate School. The VLSI layout of the driver pad used can be seen in Section K Appendix A.

3. Receiver Pad

Receiver pads are used with digital circuits to provide electrostatic discharge protection. The receiver pads used for this project were also obtained from Professor Fouts. The VLSI layout of the receiver pad used for this project can be seen in Section L Appendix A.

4. Analog Pad

Electrostatic Discharge (ESD) pads are used with analog inputs and outputs to provide electrostatic discharge protection. The ESD pads used for this project were similarly obtained from Professor Fouts. The VLSI layout of the ESD pad used for this project can be seen in Section M Appendix A.

E. VLSI FLOOR PLAN

The area that the chip is to occupy must also be laid out in the same manner that the circuits are designed. To effectively carry out the fabrication of the designed chip, significant considerations for the floor plan configuration was necessary.

1. Planning Considerations

The first consideration in deciding how this chip should be configured was what components were necessary in order to possess adequate parts to construct a switched capacitor GIC filter. Recall from Chapter II that a minimum of two OPAMPs, four switched capacitor networks, two capacitors, and one two phase non-overlapping clock are necessary. The minimum number of individual parts that MOSIS will deliver for a custom Vitesse process is 20. This would then provide 20 parts of every circuit that was placed on the chip floor plan. Since none of these components have been fabricated to date, one of the stated purposes of this research was to be able to individually evaluate each component in the GIC filter. Additionally, another purpose of this research was to set the foundation for further research to progress this design to a programmable filter which would use binary digital logic to select the various filter configurations and Q-

factor. With these purposes in mind the necessary components were made and are listed in Table 7.3.

OPAMP	Switched Capacitor Network
Two Phase Non-Overlapping Clock	Clock Output Amplifier
NOR Gate	Inverter
4xInverter	Capacitor
DFET	EFET

Table 7.3 Chip Component List

The parts chosen was based on absolute need as well as the ability to provide "back up" components. The NOR gate, inverter, 4x inverter, capacitor, DFET and EFET were selected in order to provide this back up capability in the event difficulties were encountered with the clock or switched capacitor network. The NOR gate and an inverter were selected to be used for the construction of the logic circuits for the follow-on programmable filter. They would also be necessary for the construction of a two phase non-overlapping clock should the stand alone clock have difficulties. The capacitor, DFET and EFET could be used to construct a switched capacitor network. The DFET and EFET could also be used to construct additional logic if necessary. The redundancy of components in this project was deemed necessary since this was a first attempt at constructing many of these components in GaAs.

A final major planning consideration was how much chip area would be necessary to fabricate this project. Obviously, the greater the chip area the greater the cost will be. Again the philosophy behind this decision was simple. Since this was a first attempt, a primary objective was to minimize cost. The minimum size chip area available through

the Vitesse process is 5.292 sq. mm. Smaller projects than this may be submitted but the charge will be for at least 5.292 sq. mm. This being the case initial design effort was done maximizing the available area.

2. Pad Placement

The pad placement requirements eventually determined the minimum size of the chip. As was mentioned earlier MOSIS chip packaging has a requirement of pads being at a minimum of 100 um on each side. Additionally it is required that each pad be separated by at least 100um and be at least 50 um from a corner. These requirements alone would permit at most a 36 pad chip with nine pads per side. Not surprisingly, MOSIS possessed a 36 pin package which would easily accommodate a 5.292 sq. mm chip. Using this package configuration, pin assignments were made. The primary consideration for pin assignment was to first assign the pad power pins and circuit power pins. The next step was to assign circuit locations so as to minimize routing. As can be seen in Table 7.4 all pins available were necessary in order to fulfill the minimum number of circuit components for this project.

PIN	PAD	USE
1	PWR	PAD VDD
2	PWR	PAD VSS
3	DRIVER	INV OUT
4	RECEIVER	INV IN
5	ESD	SWCAPNET IN
6	ESD	SWCAPNET OUT
7	ESD	SWCAPNET C
8	ESD	SWCAPNET CN
9	PWR	EFET VSS
10	PWR	EFET GATE
11	PWR	EFET VDD
12	PWR	CIRCUIT VDD
13	ESD	OPAMP VIN -
14	ESD	OPAMP VIN +
15	ESD	OPAMP OUT
16	RECEIVER	4XINV IN
17	DRIVER	4XINV OUT
18	PWR	CIRCUIT VSS
19	PWR	PAD VDD
20	PWR	GND
21	PWR	CAPACITOR M1
22	PWR	CAPACITOR M2
23	RECEIVER	NOR A
24	RECEIVER	NOR B
25	DRIVER	NOR OUT
26	PWR	PAD VSS
27	PWR	DFET VDD
28	PWR	DFET GATE
29	PWR	DFET VSS
30	PWR	CIRCUIT VSS
31	ESD	CLK AMP OUT
32	ESD	CLK AMP IN
33	RECEIVER	CLOCK IN
34	DRIVER	CLOCK C
35	DRIVER	CLOCK CN
36	PWR	CIRCUIT VDD

Table 7.4 Project Pin Assignments

3. Component Placement

Component placement was driven by pin placement mentioned above. Figure 7.1 depicts a graphical description of the component placement for this project. The VLSI layout of the final chip configuration can be seen in Section N Appendix A.

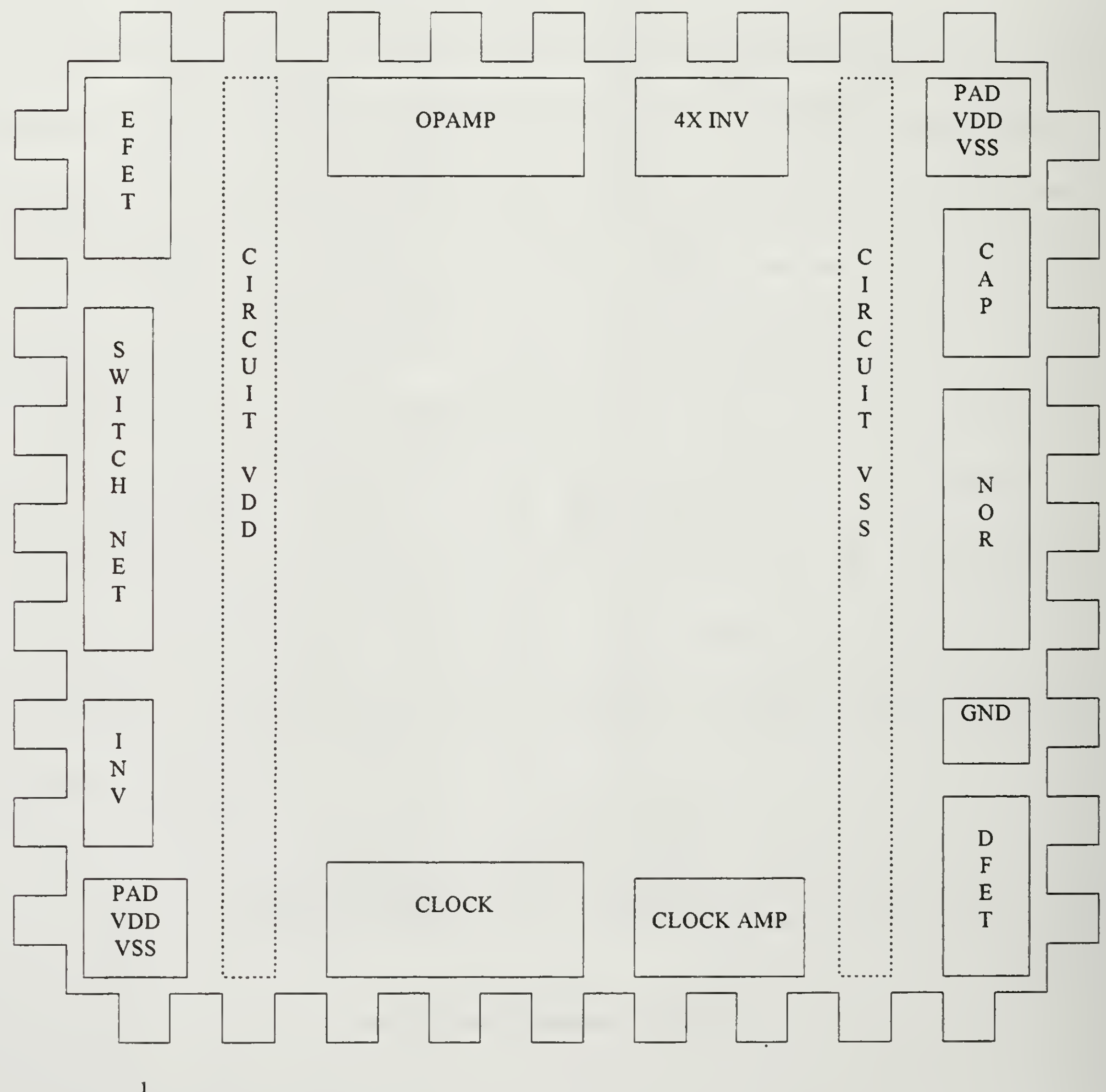


Figure 7.1 Project Chip Floor Plan

VIII. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY

The purpose of this research was to study the feasibility of the construction of a digitally programmable switched capacitor filter. The application of this device would be of great importance in the areas of signal processing, controls, and other high frequency operation communication devices. The testing of this initial engineering effort will provide insight into the performance of GaAs as a switched capacitor medium. GaAs was selected due to its higher electron mobility which permits it to operate at much higher frequencies than silicon CMOS or BiCMOS devices. Higher electron mobility will therefore allow GaAs devices to operate at higher clock speeds and thus allow the filter to have a much wider bandwidth. Lastly, GaAs possess a much higher level of radiation tolerance than silicon which makes it an ideal technology for space and military applications.

The design approach of this effort emphasized simplicity and a building block approach. Additionally, the components selected for fabrication provide backup in order to permit the construction of more complex circuits from their basic components.

B. RECOMMENDATIONS

Following fabrication, analysis of each component placed on the chip will provide insight into the performance of each and possibly show the areas in which refinement is required. Each component should be evaluated and compared to the performance data presented in this thesis. Of particular interest would be the actual maximum clock frequency of the two phase non-overlapping clock and the maximum switching frequency

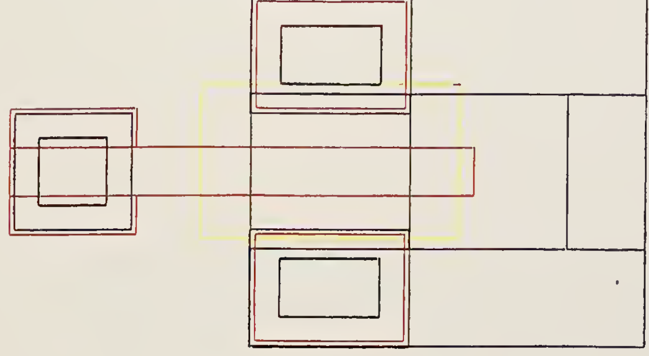
of the switched capacitor network. The fabrication of a switched capacitor GIC filter will demonstrate the feasibility of the technology. The construction of this device is the initial step in the development of an analog device capable of handling a wide range of frequencies.

Finally, the limiting feature of this research was, by far, the Magic CAD tool. Although capable in its day, Magic is by today's standards user unfriendly at best. Efforts should be pursued to either have a Vitesse HGaAs3 technology file written for the Cadence CAD tool or procurement of the COMPASS CAD tool. The latter would be preferable since it appears to be the GaAs industry "standard" and is supported by MOSIS.

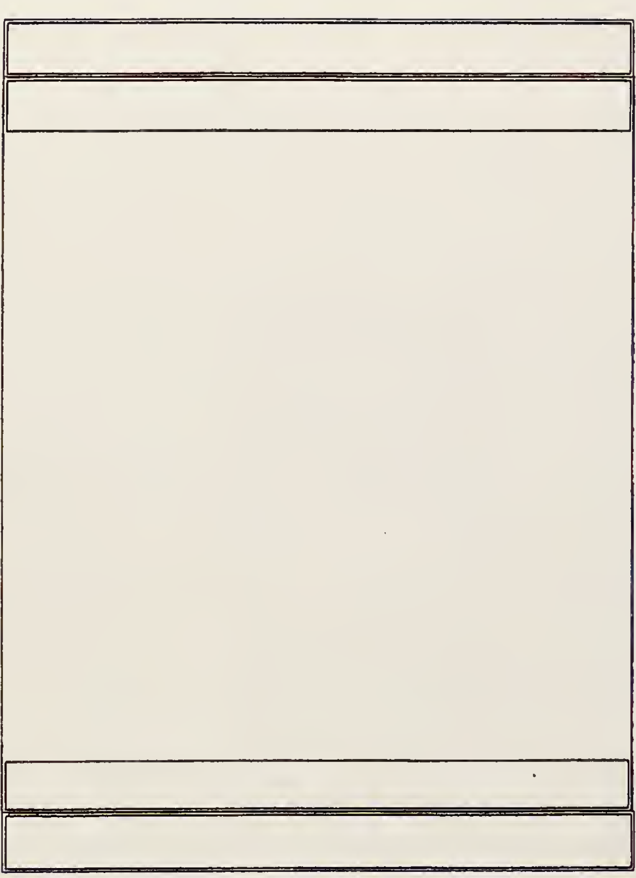
APPENDIX A. MAGIC CAD OUTPUT

This appendix contains all Magic CAD plots constructed in this thesis.

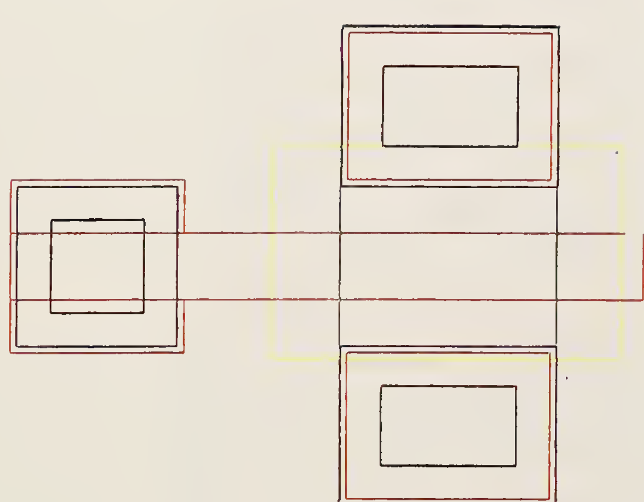
A. DIODE LAYOUT



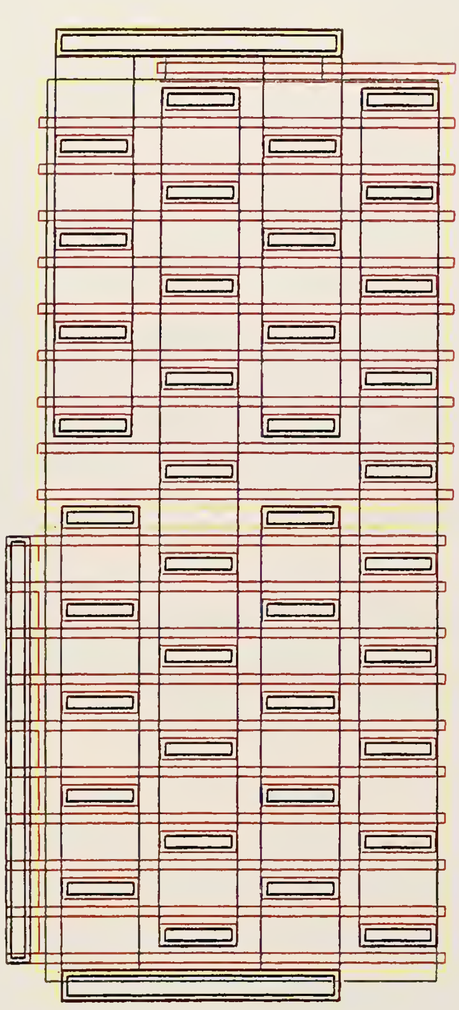
B. CAPACITOR LAYOUT



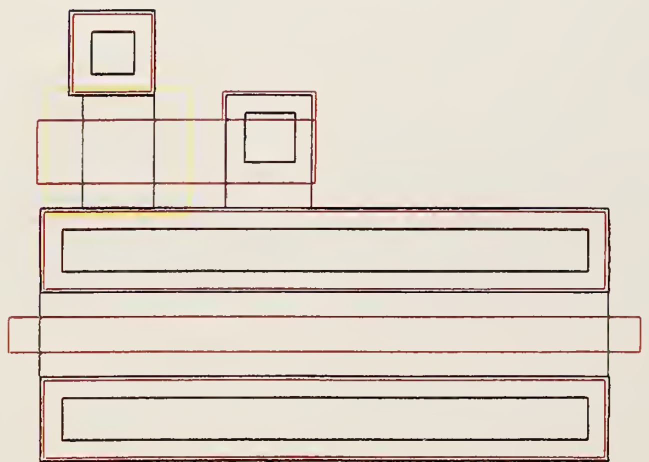
C. MESFET LAYOUT



D. MESFET LAYOUT (FINGERED)

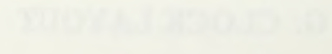


E. INVERTER LAYOUT

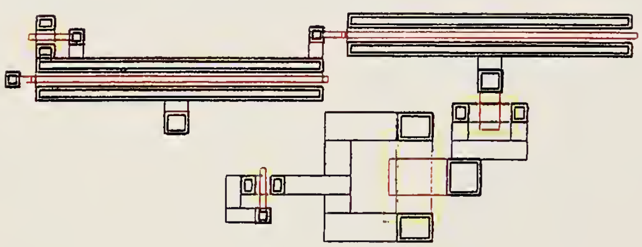


F. NOR GATE LAYOUT

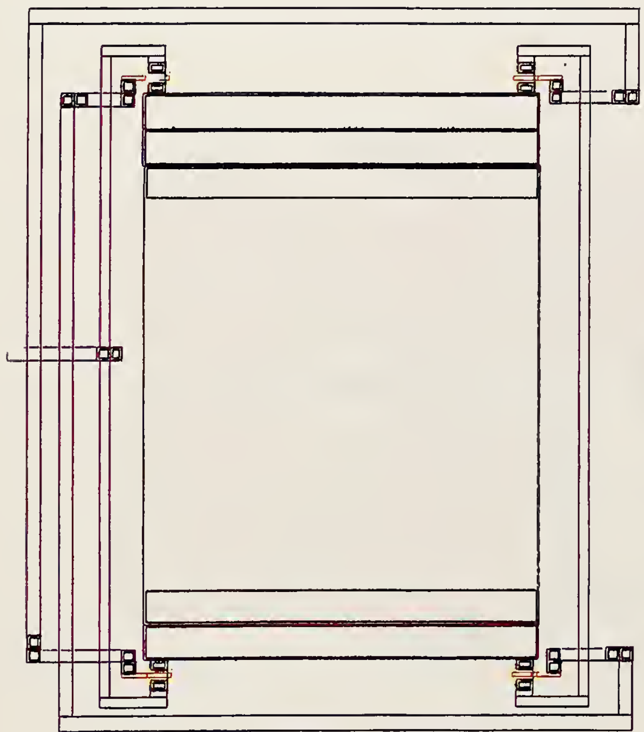
G. CLOCK LAYOUT



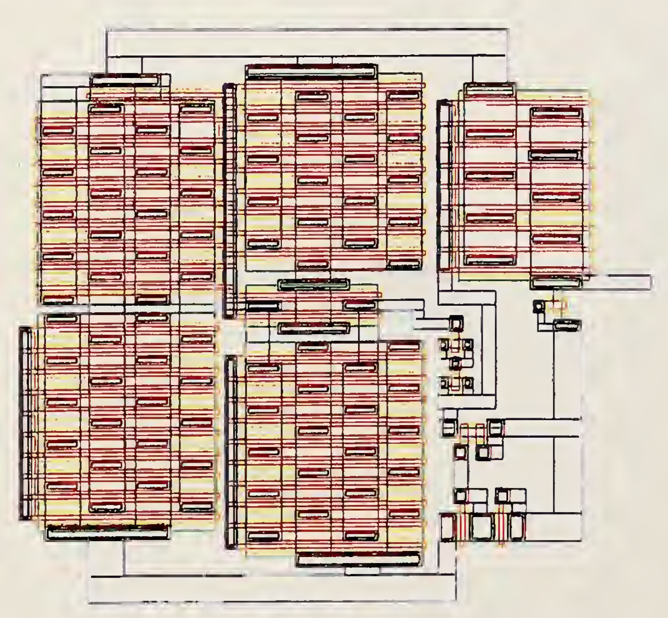
H. CLOCK AMPLIFIER LAYOUT



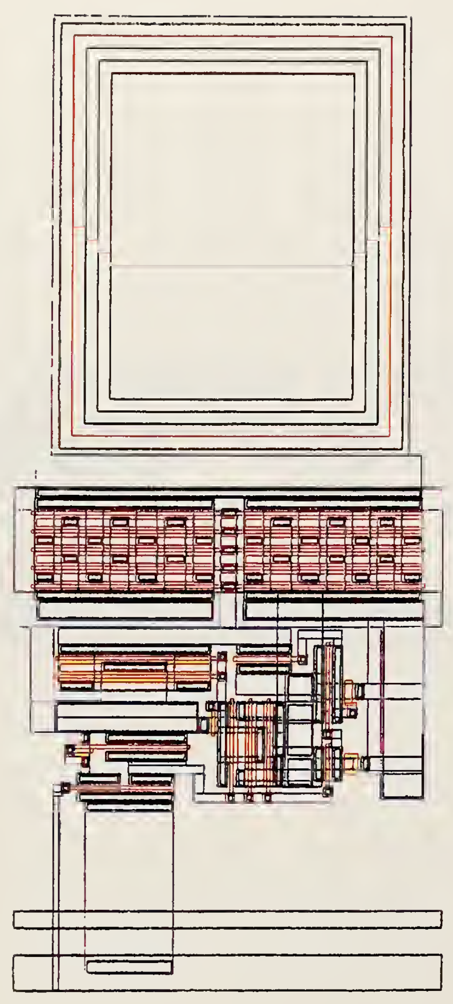
I. SWITCH CAPACITOR NETWORK LAYOUT



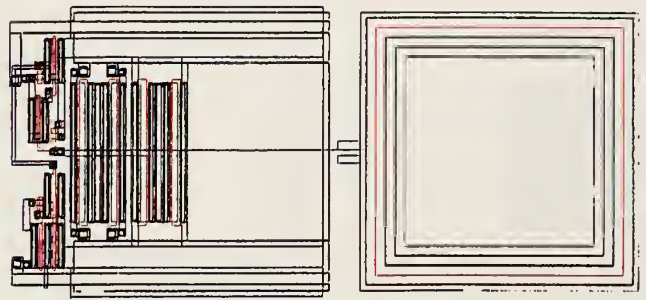
J. OPERATIONAL AMPLIFIER LAYOUT



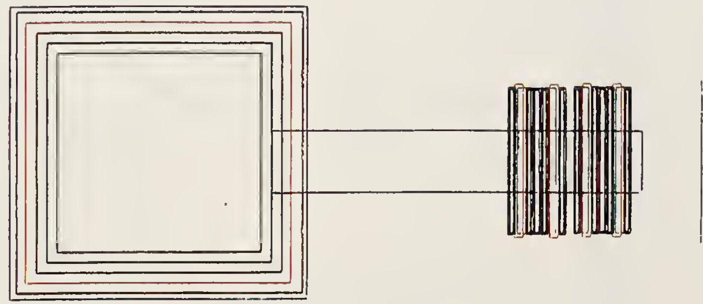
K. DRIVER PAD LAYOUT



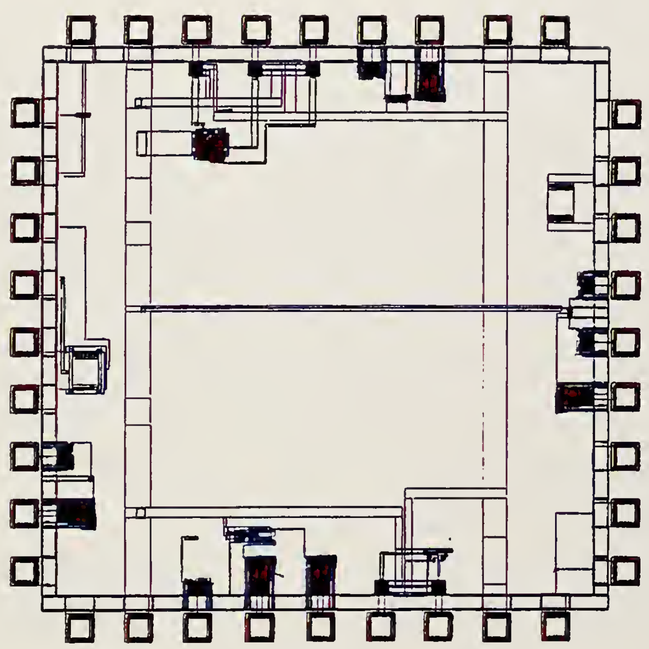
L. RECEIVER PAD LAYOUT



M. ESD PAD LAYOUT



N. PROJECT CHIP LAYOUT



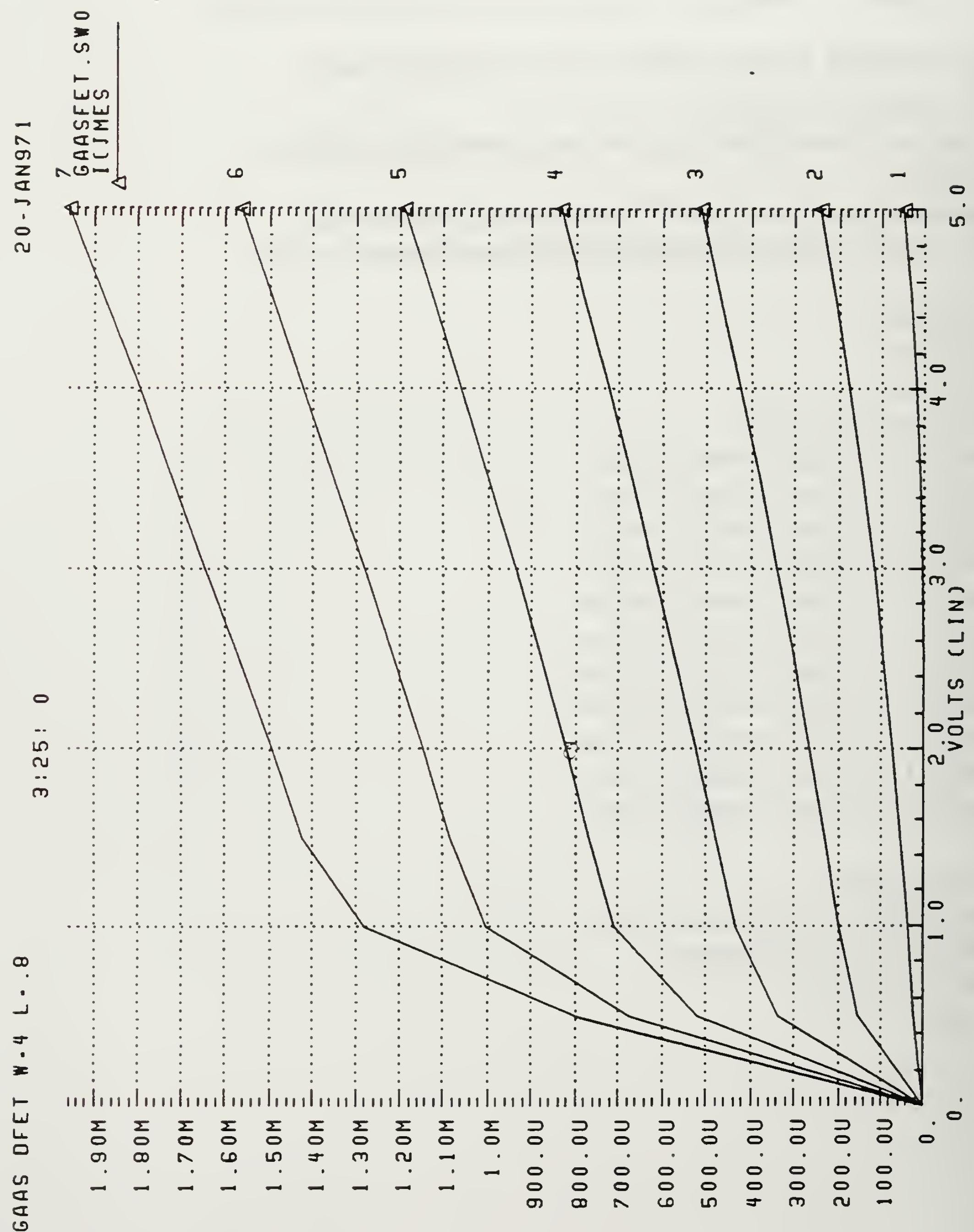
APPENDIX B. HSPICE CODE AND DATA

This appendix contains the HSpice code and data used in this thesis.

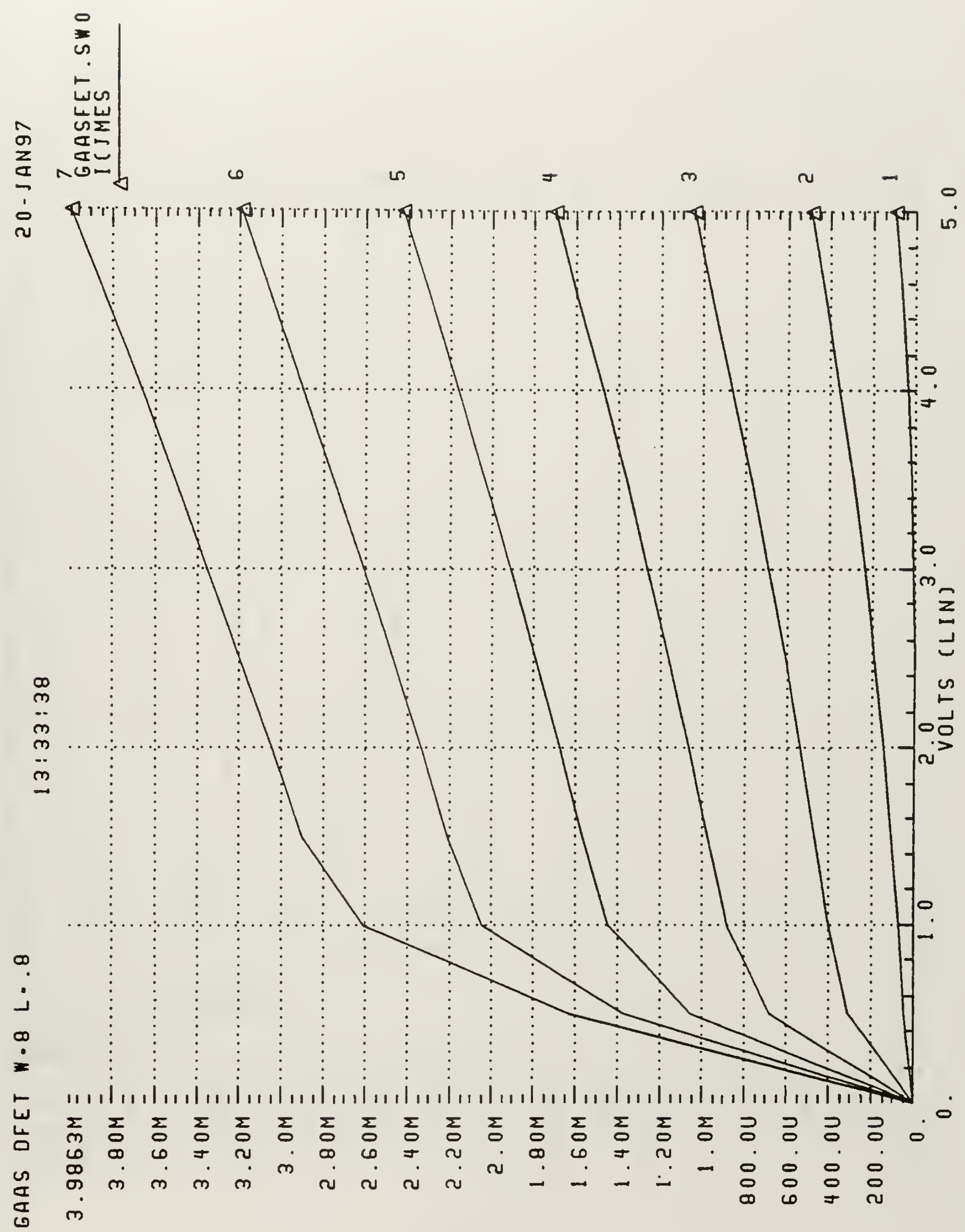
A. MESFET FAMILY OF CURVES HSPICE CODE

```
This circuit is a GaAs FET
*include Vitesse HGaAs3 models and parameters for HSPice
.protect
.include 'tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners'typical

.unprotect
VDS 1 0
VGS 2 0
*FETs to be evaluated
JMES 1 2 0 0 dpl.l W=4u L=0.8u
JMES 1 2 0 0 dpl.l W=8u L=0.8u
JMES 1 2 0 0 dpl.l W=10u L=0.8u
JMES 1 2 0 0 dpl.l W=16u L=0.8u
JMES 1 2 0 0 dpl.l W=60u L=0.8u
JMES 1 2 0 0 dpl.l W=96u L=0.8u
JMES 1 2 0 0 dpl.l W=360u L=0.8u
JMES 1 2 0 0 dpl.l W=375u L=0.8u
JMES 1 2 0 0 dpl.l W=400u L=0.8u
JMES 1 2 0 0 dpl.l W=2u L=1.6u
JMES 1 2 0 0 enh.l W=50u L=0.8u

*Analysis type
.DC VDS 0 5 0.5 VGS -1 0.7 0.25
.PROBE DC I(1) v(2) I(jmes
.OPTION POST
.END
```

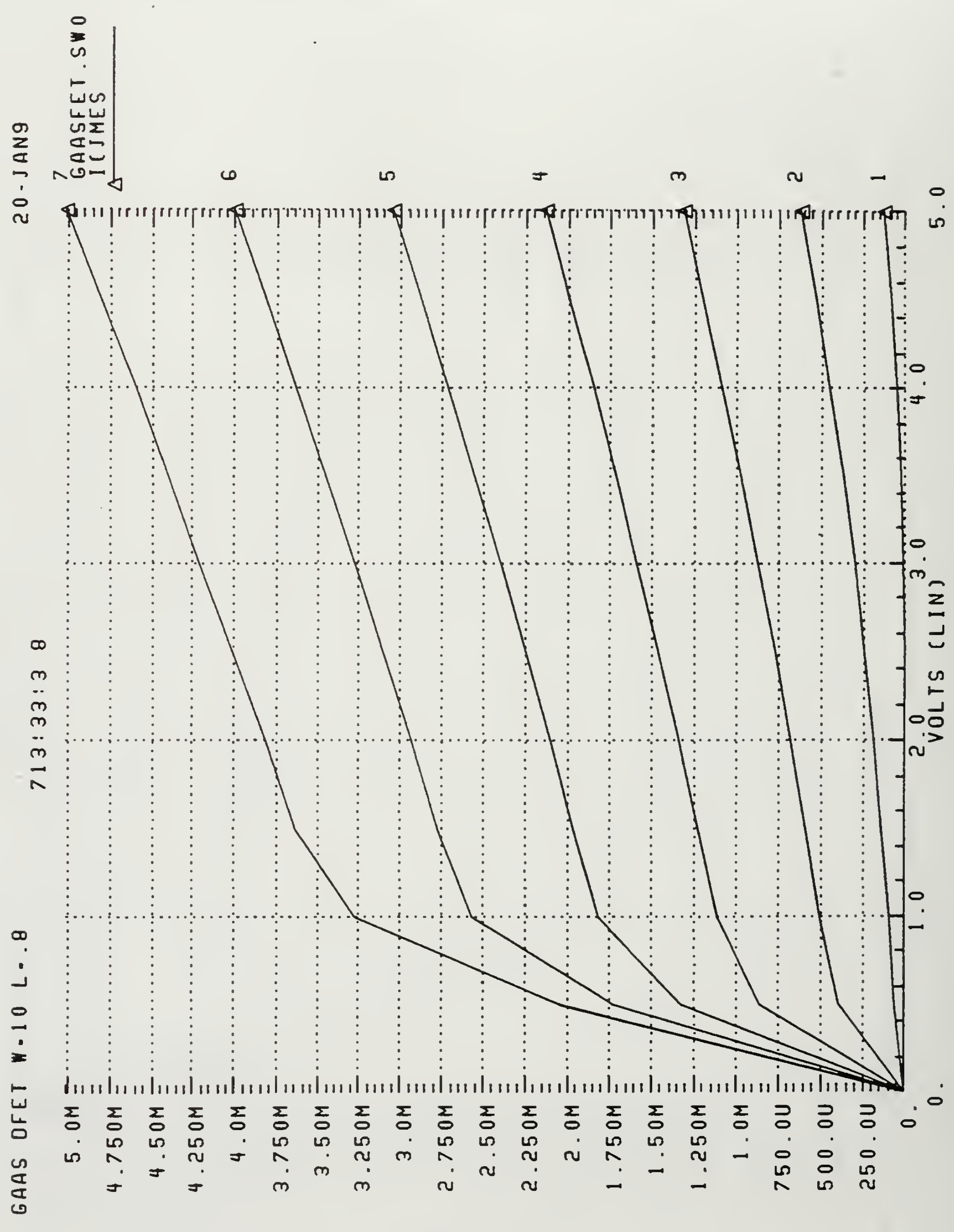
1. GaAs DFET W=4 L=0.8



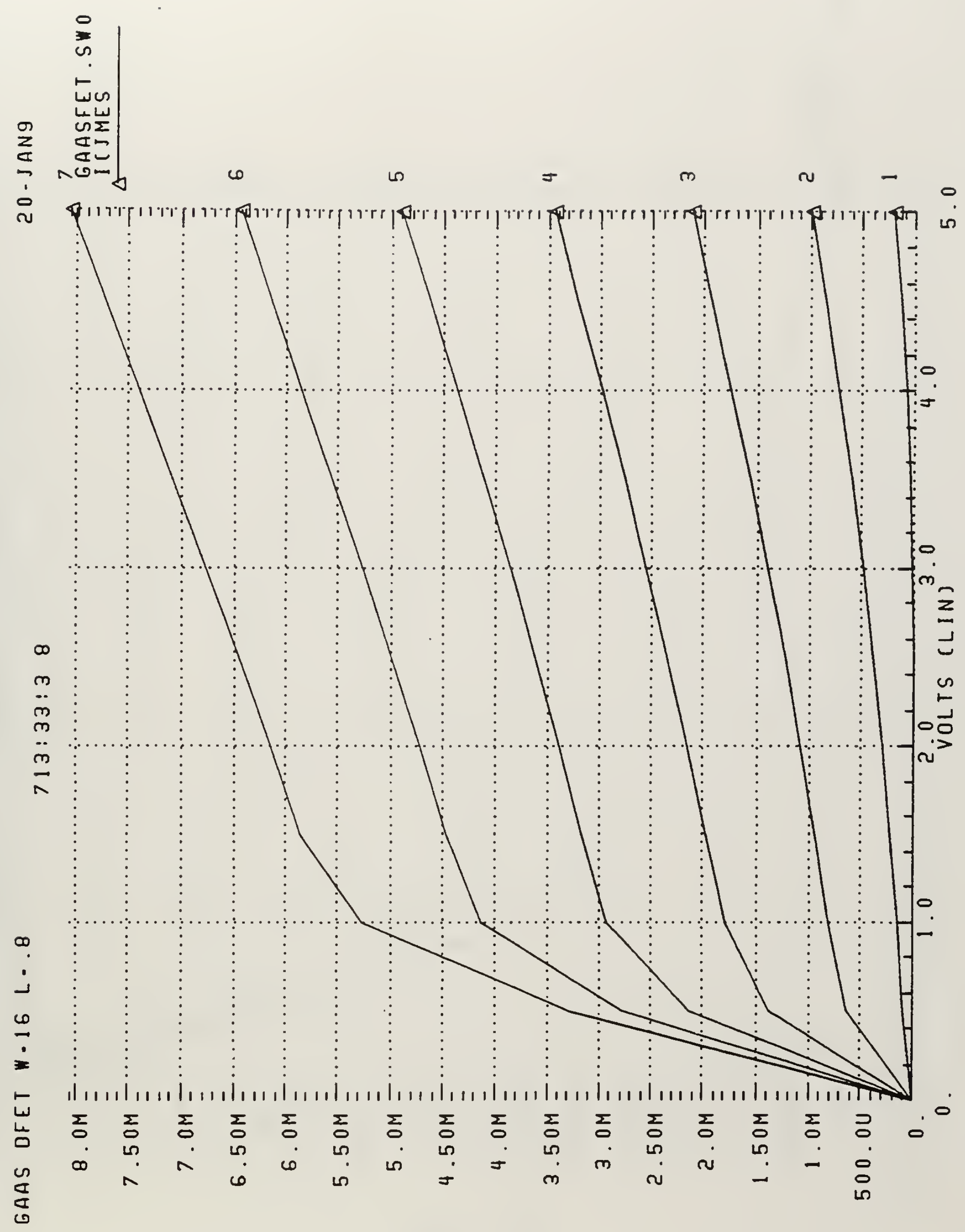
2. GaAs DFET W=8 L=0.8



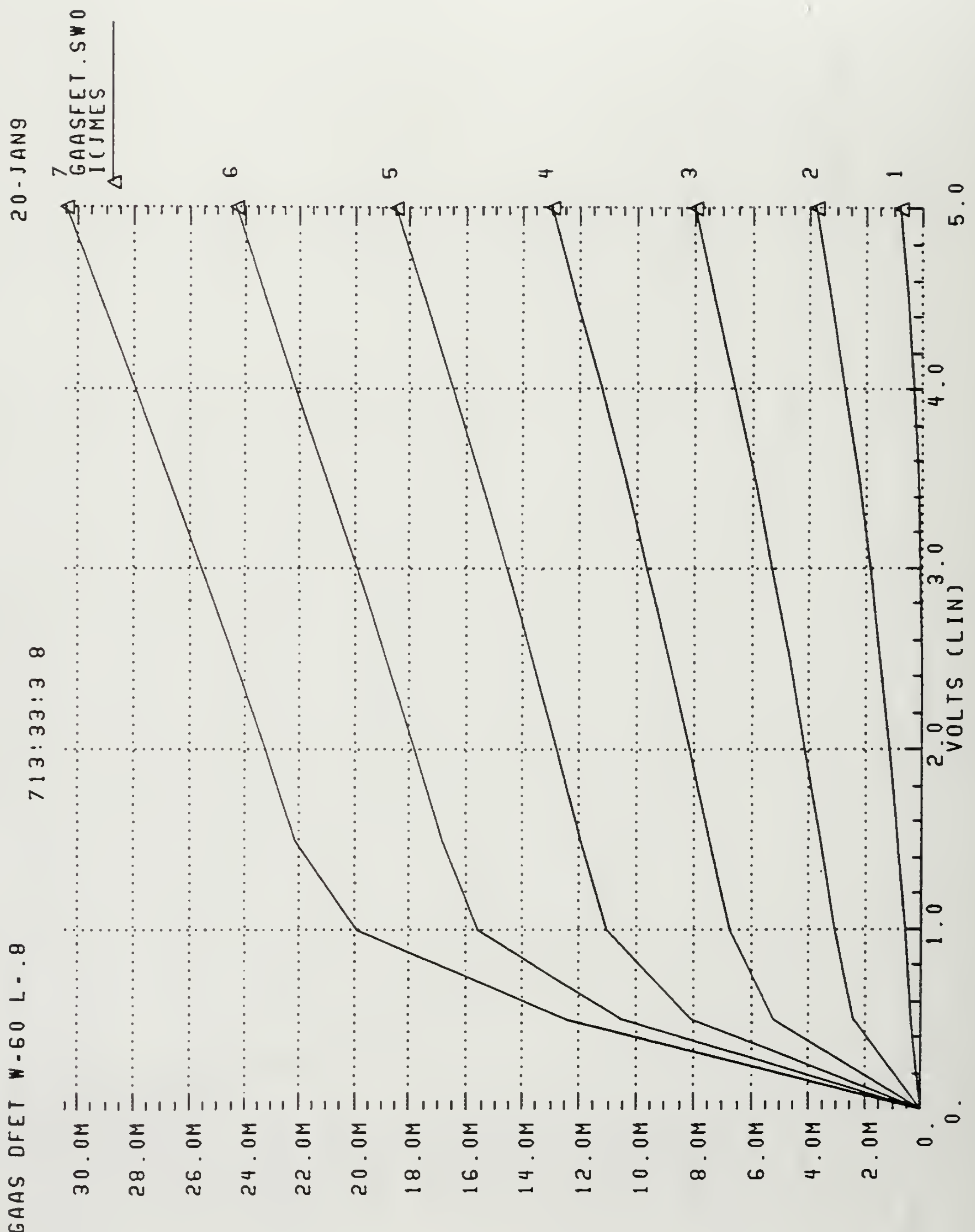
3. GaAs DFET W=10 L=0.8



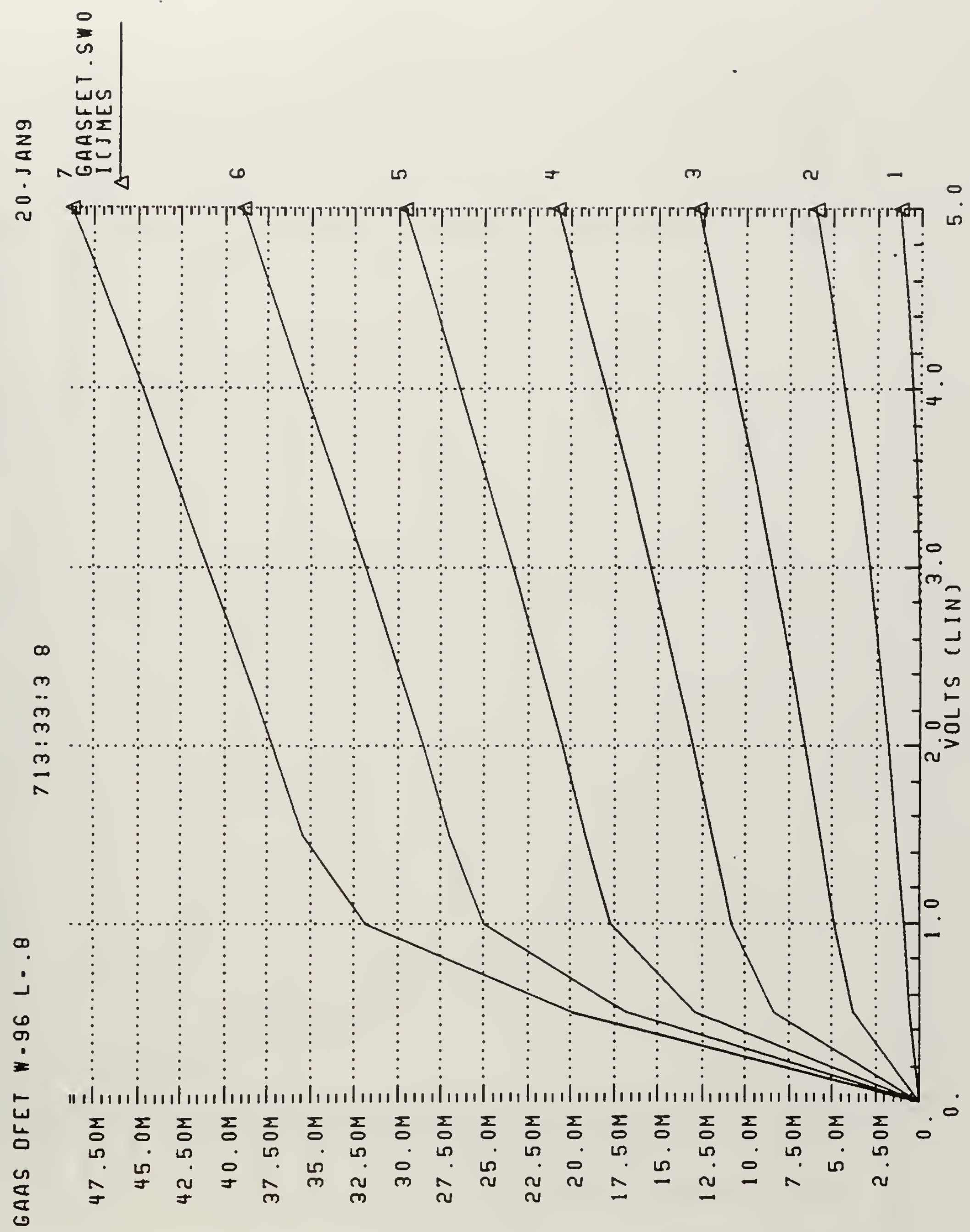
4. GaAs DFET W=16 L=0.8



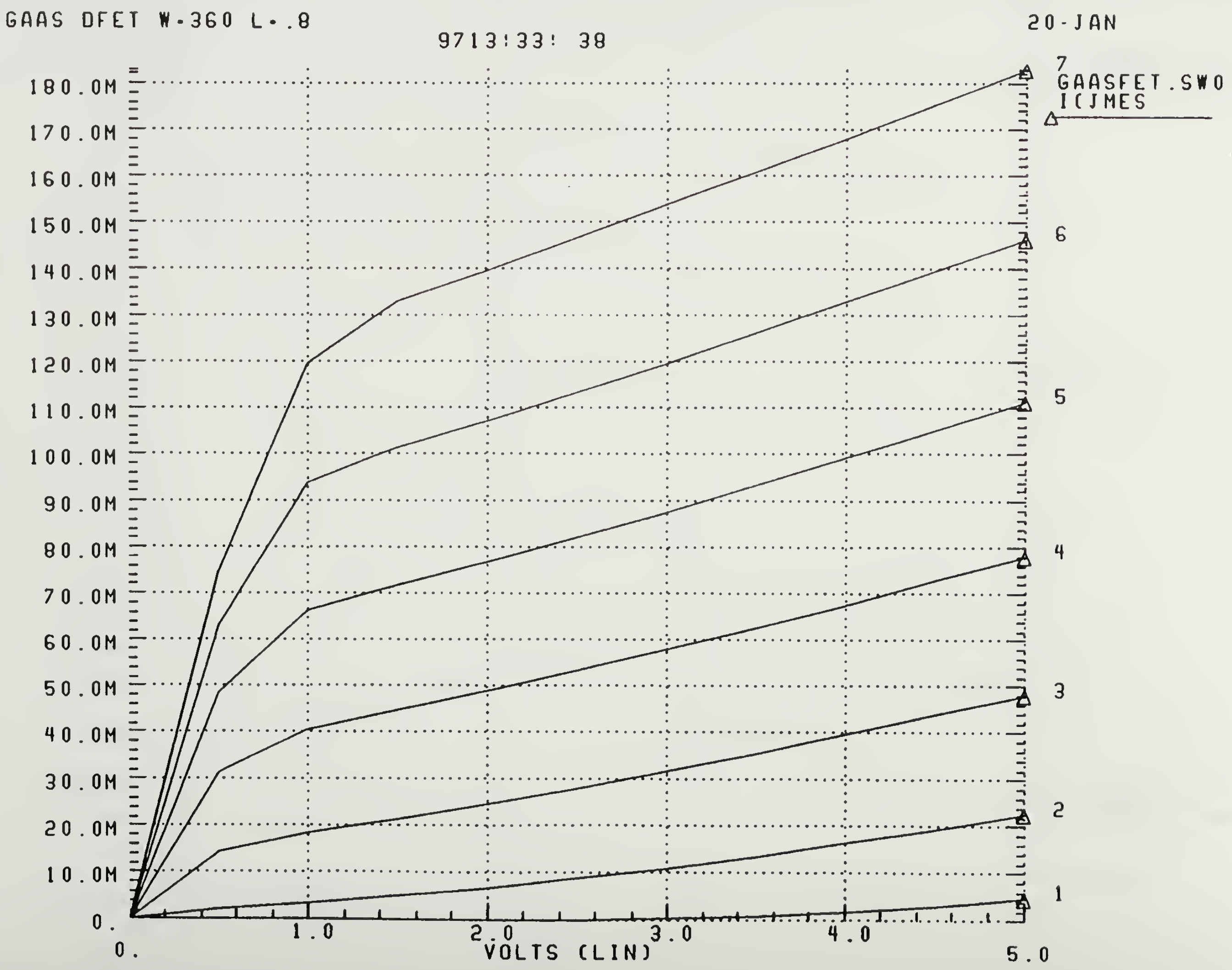
5. GaAs DFET W=60 L=0.8



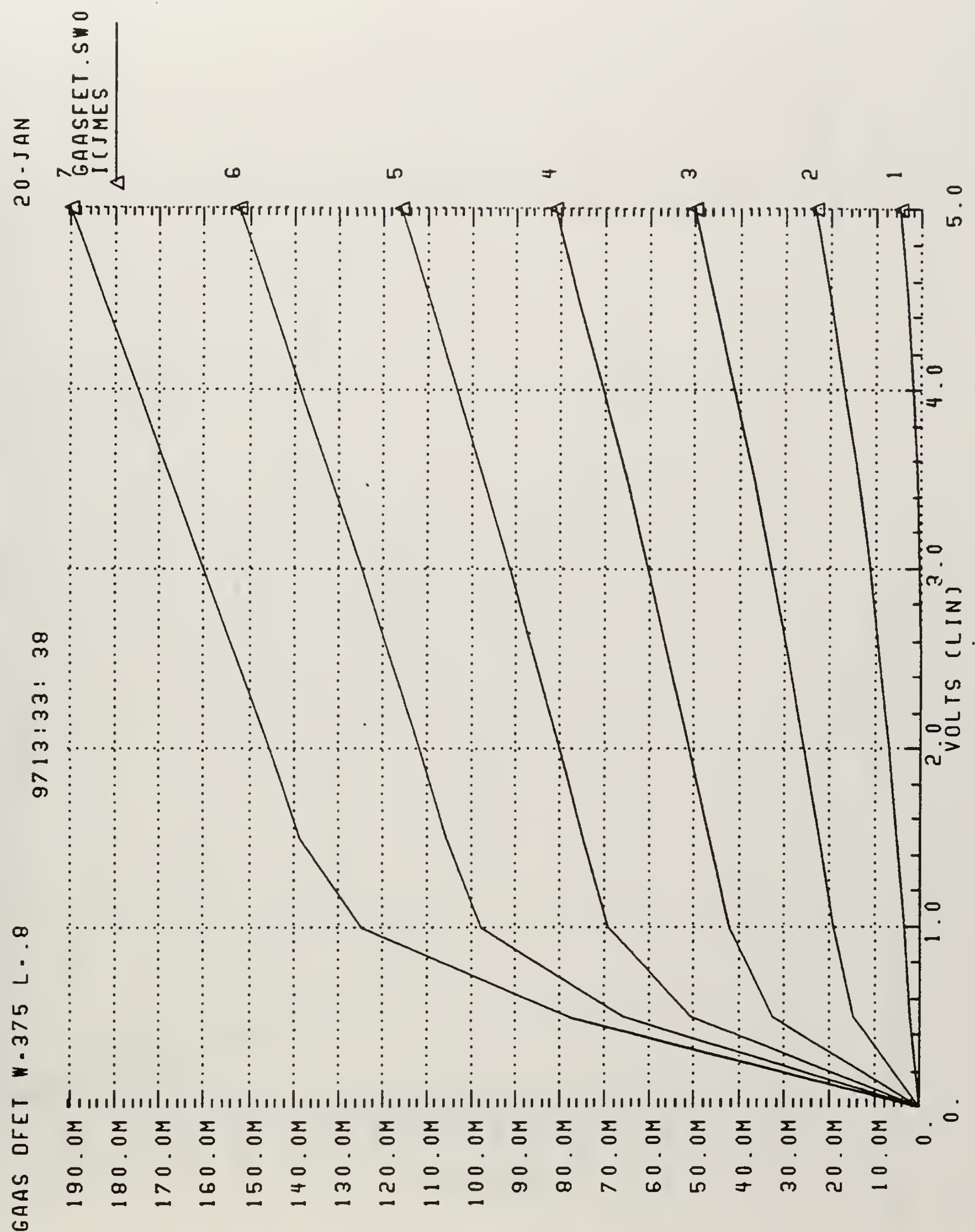
6. GaAs DFET W=96 L=0.8



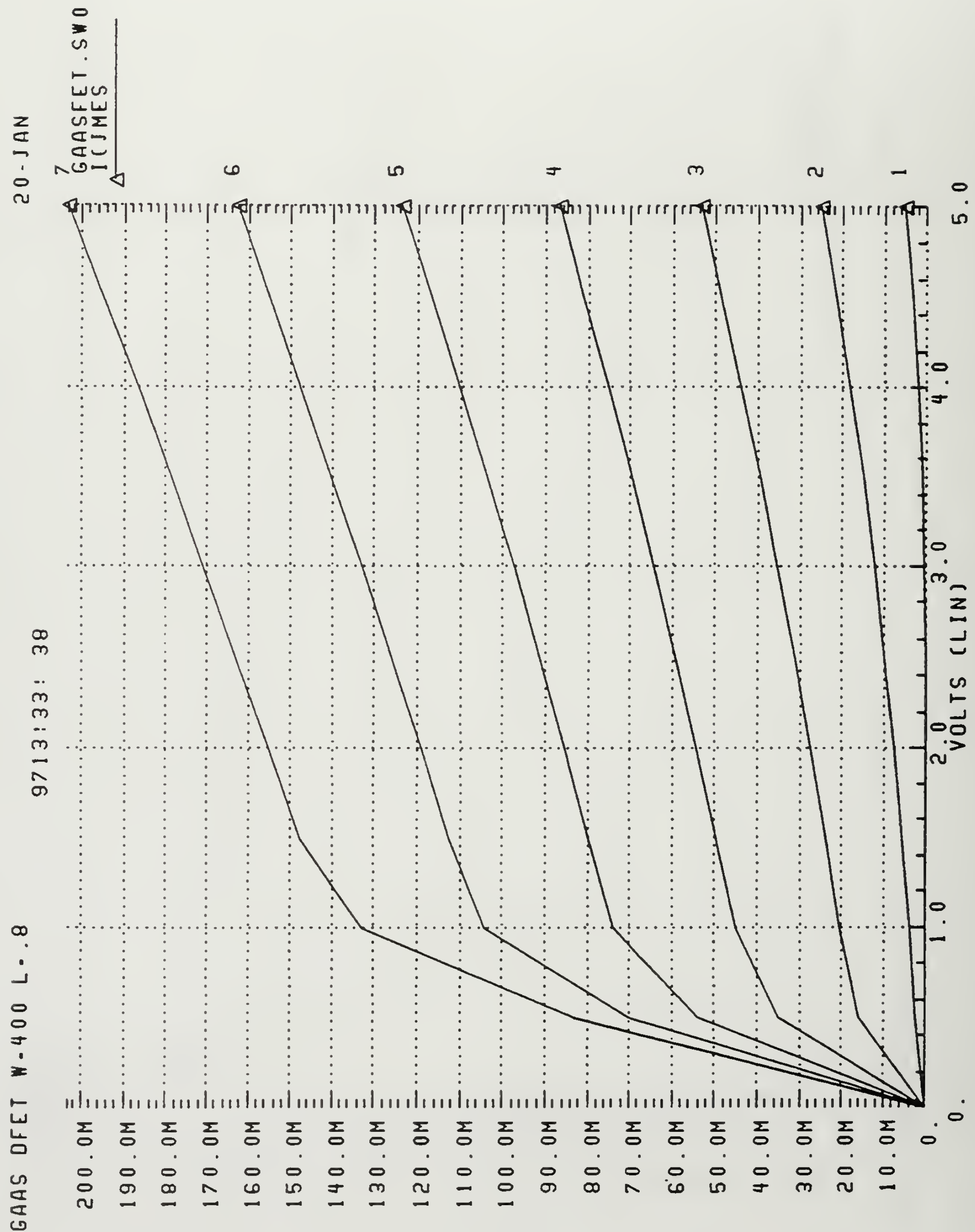
7. **GaAs DFET W=360 L=0.8**



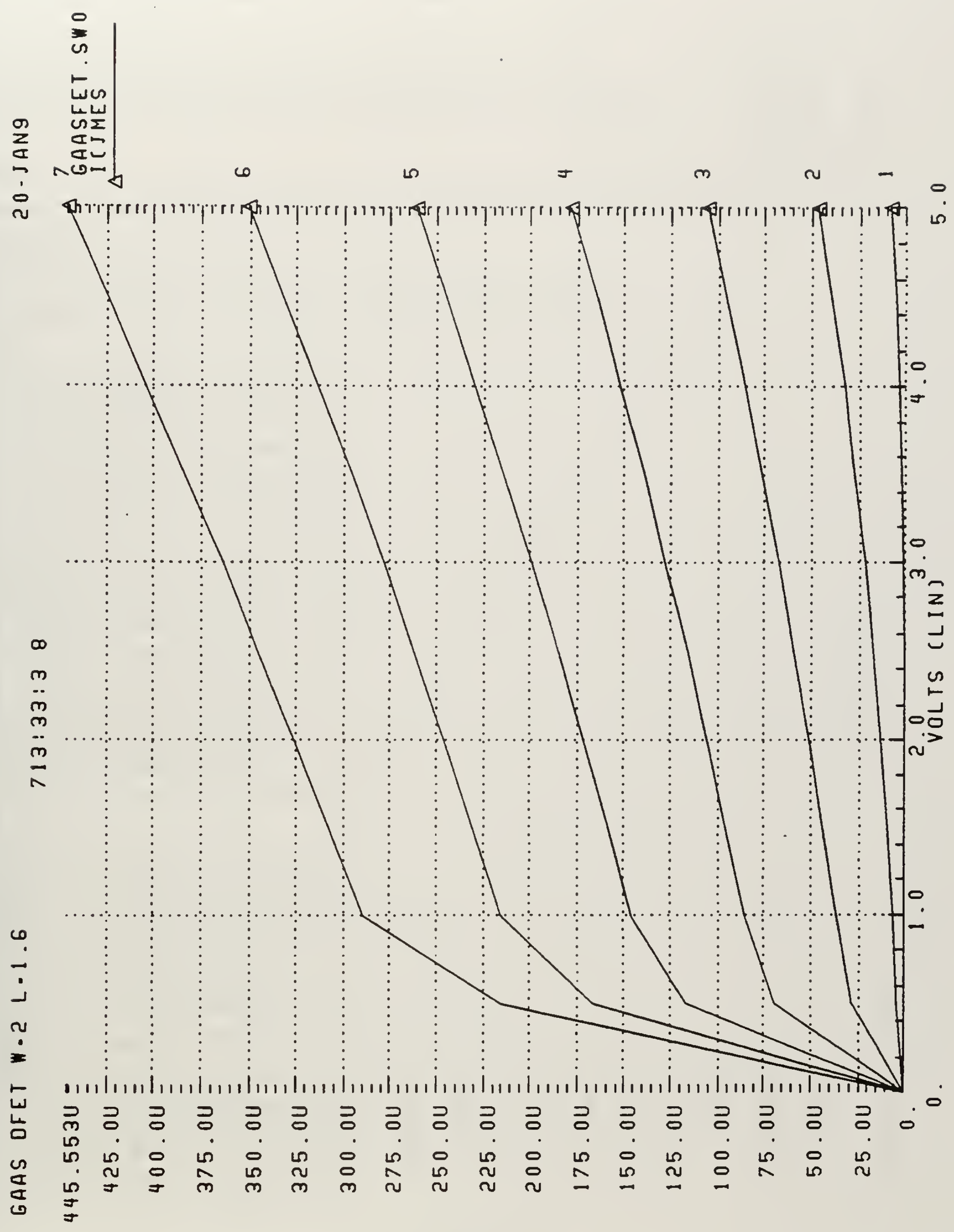
8. GaAs DFET W=375 L=0.8



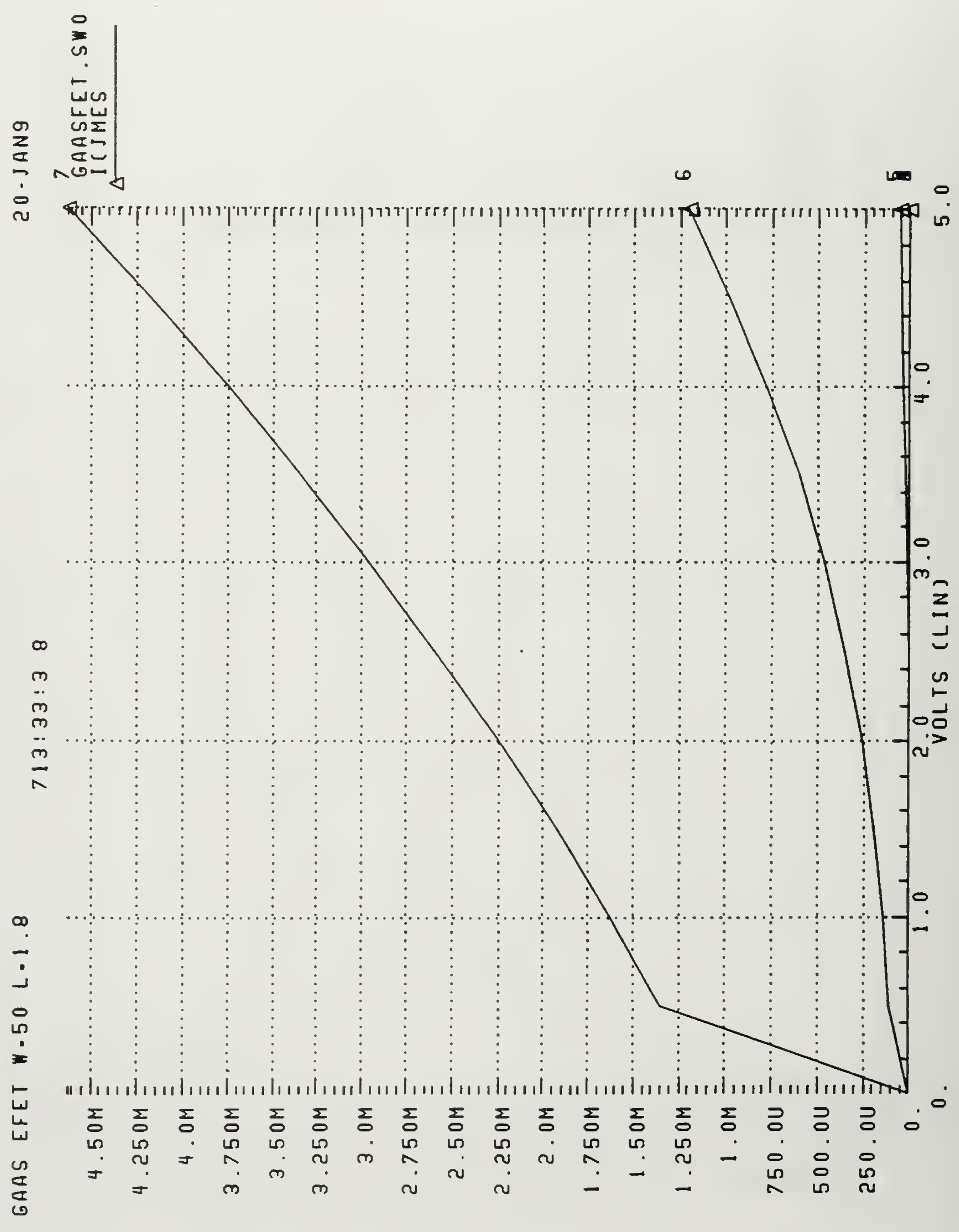
9. GaAs DFET W=400 L=0.8



10. GaAs DFET W=2 L=1.6



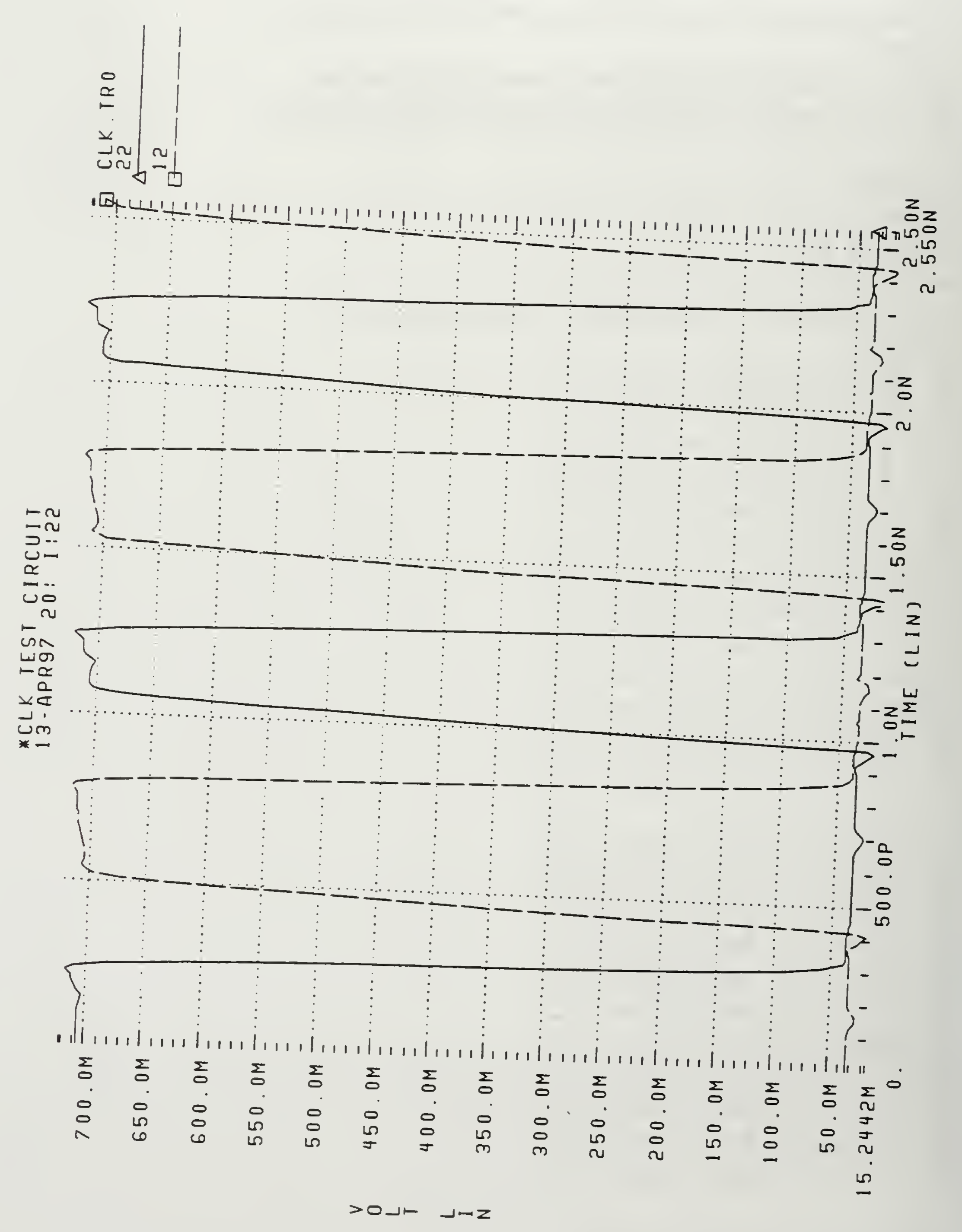
11. GAAS EFET W=50 L=1.8



B. CLOCK TEST CIRCUIT HSPICE CODE

```
*include Vitesse HGaAs3 models and parameters for HSpice
.protect
.include 'tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners'typical

.unprotect
*power
vdd 1 0 dc 5.0
vss 10 0 dc 0
vin 8 0 pulse(0V 0.7V 50 PS 150PS 150PS 350PS 1000PS)
*circuit
j8    1 21 21 10  dpl.2 l=1.0 w=  1.2
j9   21   8 10 10  enh.1 l=0.8 w=23.5
j10    1 14 14 10  dpl.2 l=1.0 w=  1.2
j11    8   8 10 10  enh.1 l=0.8 w=23.5
j12  14 12 10 10  enh.1 l=0.8 w=23.5
j13    1 16 16 10  dpl.2 l=1.0 w=  1.2
j14  18 16 10 10  enh.1 l=0.8 w=23.5
j15    1 18 18 10  dpl.2 l=1.0 w=  1.2
j16  18 16 10 10  enh.1 l=0.8 w=23.5
j17    1   2   2 10  dpl.2 l=1.0 w=  1.2
j18  21   8 10 10  enh.1 l=0.8 w=23.5
j19    1 22 22 10  dpl.2 l=1.0 w=  1.2
j2    22   2 10 10  enh.1 l=0.8 w=23.5

j20    1 24 24 10  dpl.2 l=1.0 w=  1.2
j21    24  21 10 10  enh.1 l=0.8 w=23.5
j22  24 22 10 10  enh.1 l=0.8 w=23.5
j23    1 26 26 10  dpl.2 l=1.0 w=  1.2
j24  28 26 10 10  enh.1 l=0.8 w=23.5
j25    1 28 28 10  dpl.2 l=1.0 w=  1.2
j26  28 26 10 10  enh.1 l=0.8 w=23.5
j27    1   3   3 10  dpl.2 l=1.0 w=  1.2
j28    3 28 10 10  enh.1 l=0.8 w=23.5
j29    1 12 12 10  dpl.2 l=1.0 w=  1.2
j3    12   2 10 10  enh.1 l=0.8 w=23.5

.options dcon=1 scale=1E-06 post
.trans 10ps 2550ps
.end
```

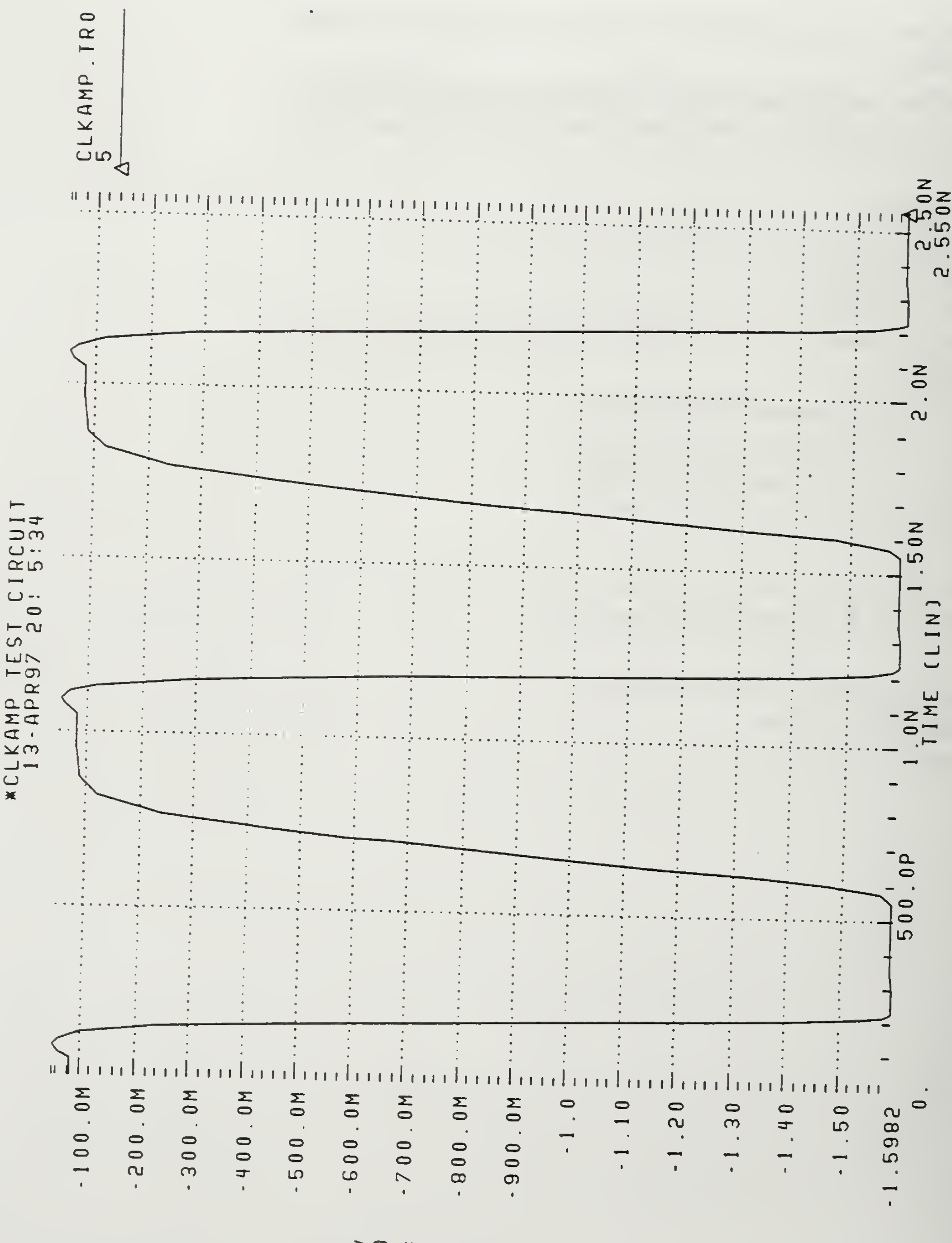
1. Clock Test Circuit Performance



C. CLOCK AMPLIFIER CIRCUIT HSPICE CODE

```
*include Vitesse HGaAs3 models and parameters for HSpice
.protect
.include 'tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners'typical

.unprotect
*power
vdd 1 0 dc 5.0
vss 10 0 dc -5.0
vin 8 0 pulse(0.1V 0.7V 50 PS 150PS 150PS 350PS 1000PS)
*circuit
j1   1  2   2 10  dpl.2  l=0.8 w=  3.0
j2   2  8   0 10  enh.1 l=0.8 w=50.0
j3   1  2   3 10  enh.1 l=0.8 w=50.0
j4   5 10 10 10  dpl.2  l=0.8 w=  3.0

jdi1  4  3  4  10  dpl.1 l=  3.0 w=  3.0
jdi2  5  4  5  10  dpl.1 l=25.0 w=25.0

.options dcon=1 scale=1E-06 post
.trans 10ps 2550ps
.end
```

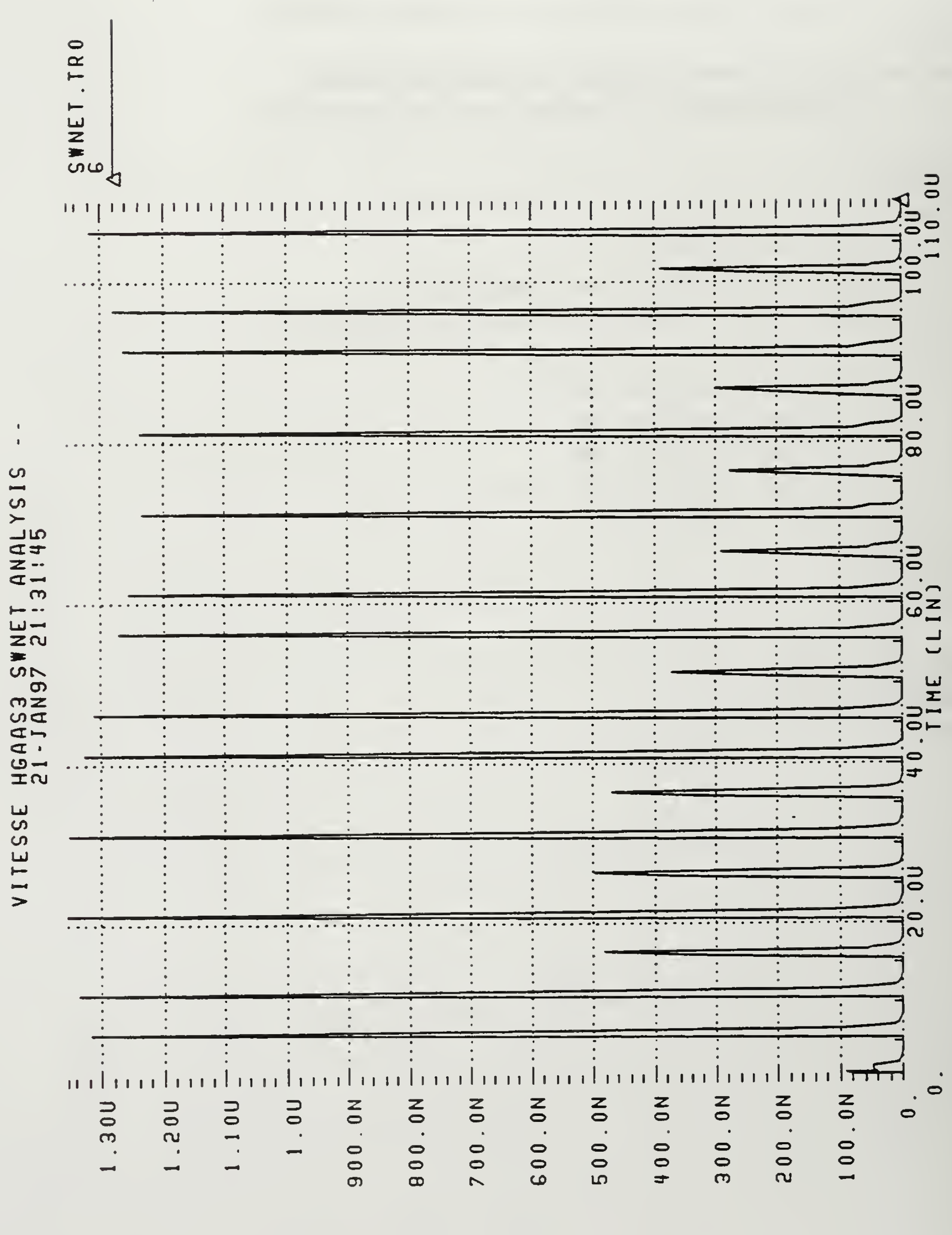
1. Clock Amplifier Circuit Performance



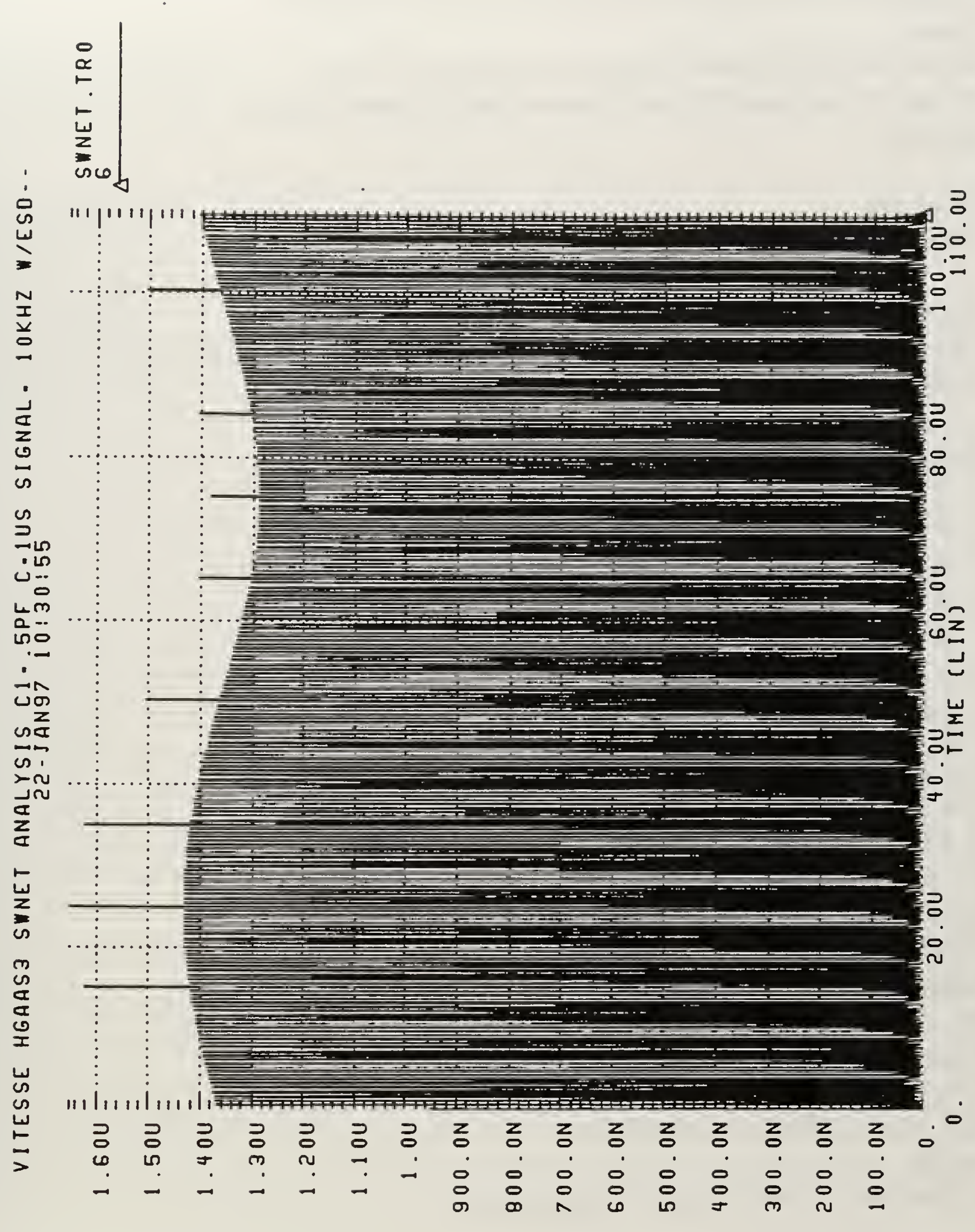
D. SWITCHED CAPACITOR NETWORK HSPICE CODE

```
*include Vitesse HGaAs3 models and parameters for HSpice
.protect
.include 'tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners'typical

.unprotect
*power
vdd 1 0 sin(2.5 0.5 10k 0 0)
vc  2 0  pulse(-1.5 -0.1 .05us .15us .15us .35us 1us)
vcn 3 0 pulse(-1.5 -0.1 .55us .15us .15us .15us .35us 1us)
*circuit
j1   1  2   4 0  dpl.1  l=0.8 w=  4.0
j2   2  3   5 0  dpl.1  l=0.8 w=  4.0
j3   4  3   6 0  dpl.1  l=0.8 w=  4.0
j4   5  2   6 0  dpl.1  l=0.8 w=  4.0

c1 4 5 .5pf
r1 6 0 100M

.trans 10us 110ps
.option dcon=1 post
.end
```

1. Switch Capacitor Network Performance 10X



2. Switch Capacitor Network Performance 100X

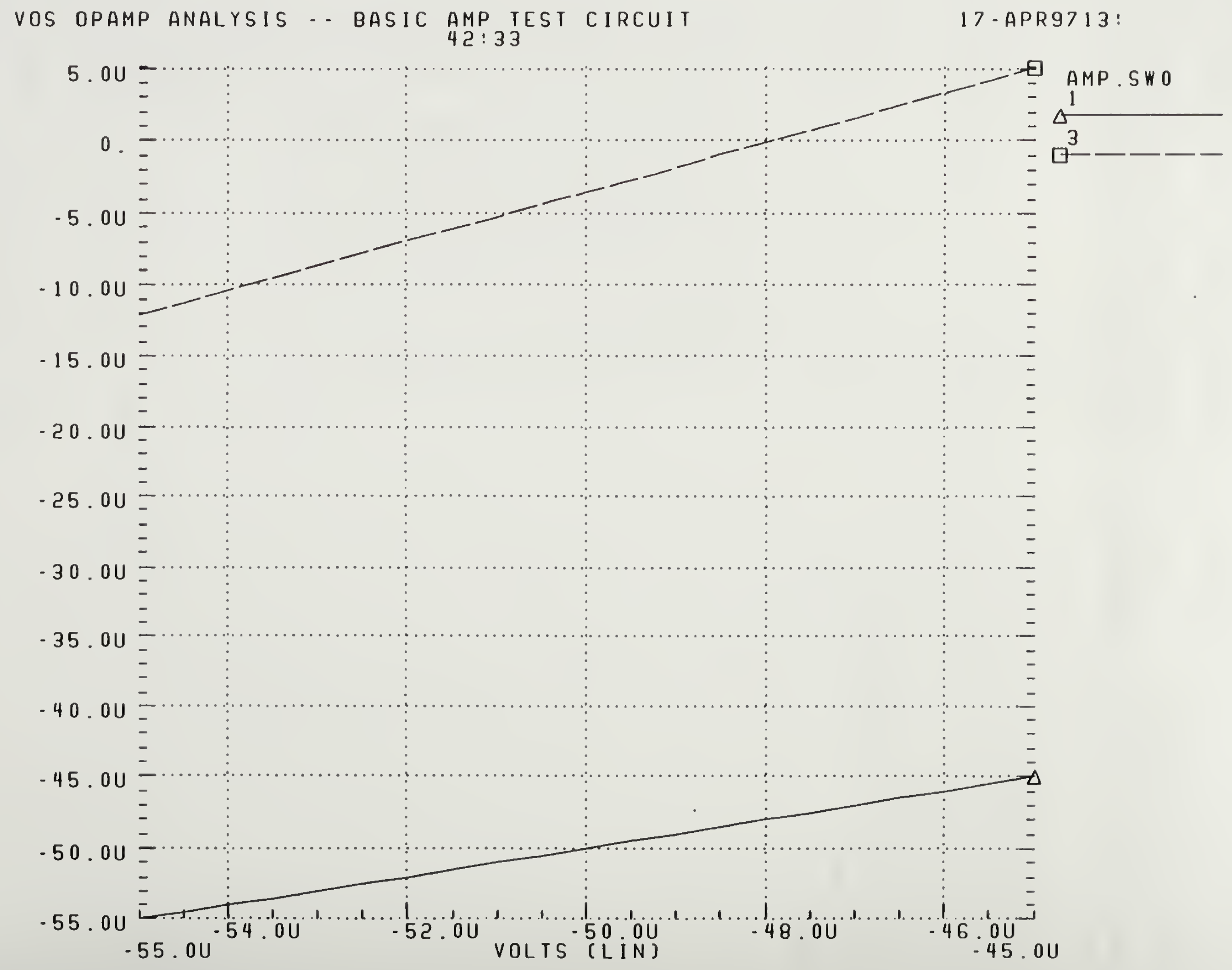


E. OPAMP HSPICE CODE

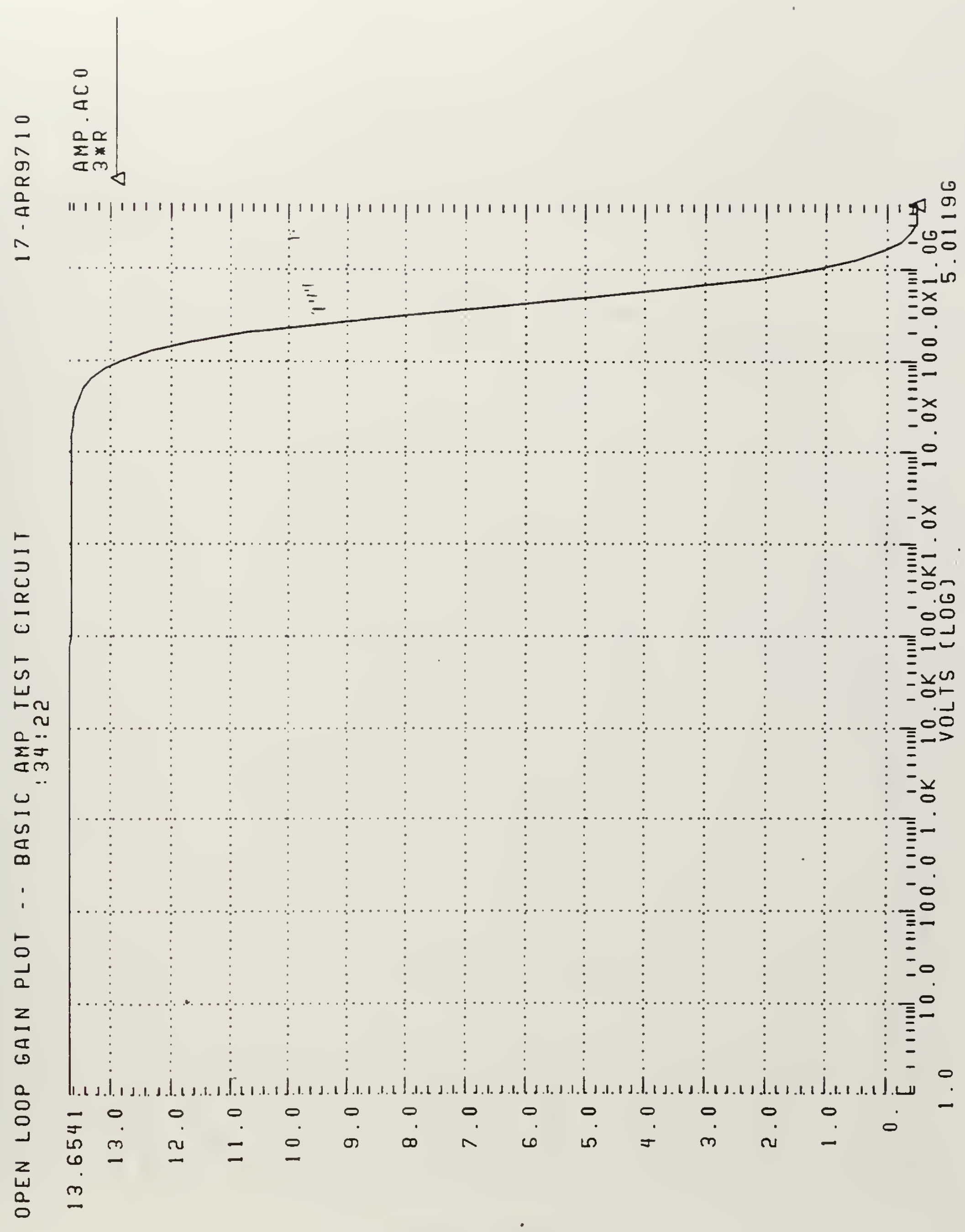
```
*include Vitesse HGaAs3 models and parameters for HSpice
.protect
.include 'tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners'typical
.unprotect

*Subcircuit
.SUBCKT gaasamp 1 2 7

*power
vdd 6 0 dc 5.0
vss 10 0 dc -5.0

*circuit
j1   4  1  3 10   dpl.1  l=0.8 w=  40.0
j2   5  2  3 10   dpl.1  l=0.8 w= 400.0
j3   6  5  4 10   dpl.1  l=0.8 w= 375.0
j4  16  5  5 10   dpl.1  l=0.8 w=  60.0
j5   6  5 16 10   dpl.1  l=0.8 w=  36.0
j6   3  9  9 10   dpl.1  l=0.8 w=  16.0
j7   9 10 10 10   dpl.1  l=0.8 w=  16.0
j8  12  9 15 10   dpl.1  l=1.6 w=   2.0
j9  15 10 10 10   dpl.1  l=1.6 w=   2.0
j10  6 12  7 10   dpl.1  l=0.8 w=  96.0
j11  7 10 10 10   dpl.1  l=0.8 w=  10.0
jd1    11  5 11 10  dpl.1  l=1.6 w=  2.0
jd2    11 11 12 10  dpl.1  l=1.6 w=  2.0
.ends gaasamp
**Main Circuit**
xamp 1 2 3 gaasamp
**Test Circuits**
**Openloop Gain and Phase Test, Use .AC and .probe**
vinp 0 100 AC SIN(0 1m 100x 0 0)
vinm 2 0
vos 1 100 DC 44.284u $output offset voltage

**CMRR Test, Use .AC and .probe**
Vcm 100 0AC SIN(0 1m 100x 0 0)
Vn 100 2
Vp 100 1

**Offset Voltage Test, Use .DC**
```

```
r1 2 0 1k
r2 3 2 1k
Vos 1 0

**Sr Test, Use .TRAN**
vinp 1 0 pulse(-1m 1m 0 1n 1n 5e-8 1e-7)
vinm 2 3

**Control Analysis
.DC Vos -55 -45 .5u
.AC DEC 10 1 4g
.TRAN 1p 0.060u
.probe v(1) v(2) v(3) i(1) i(2) i(3)
.option post
.end
```

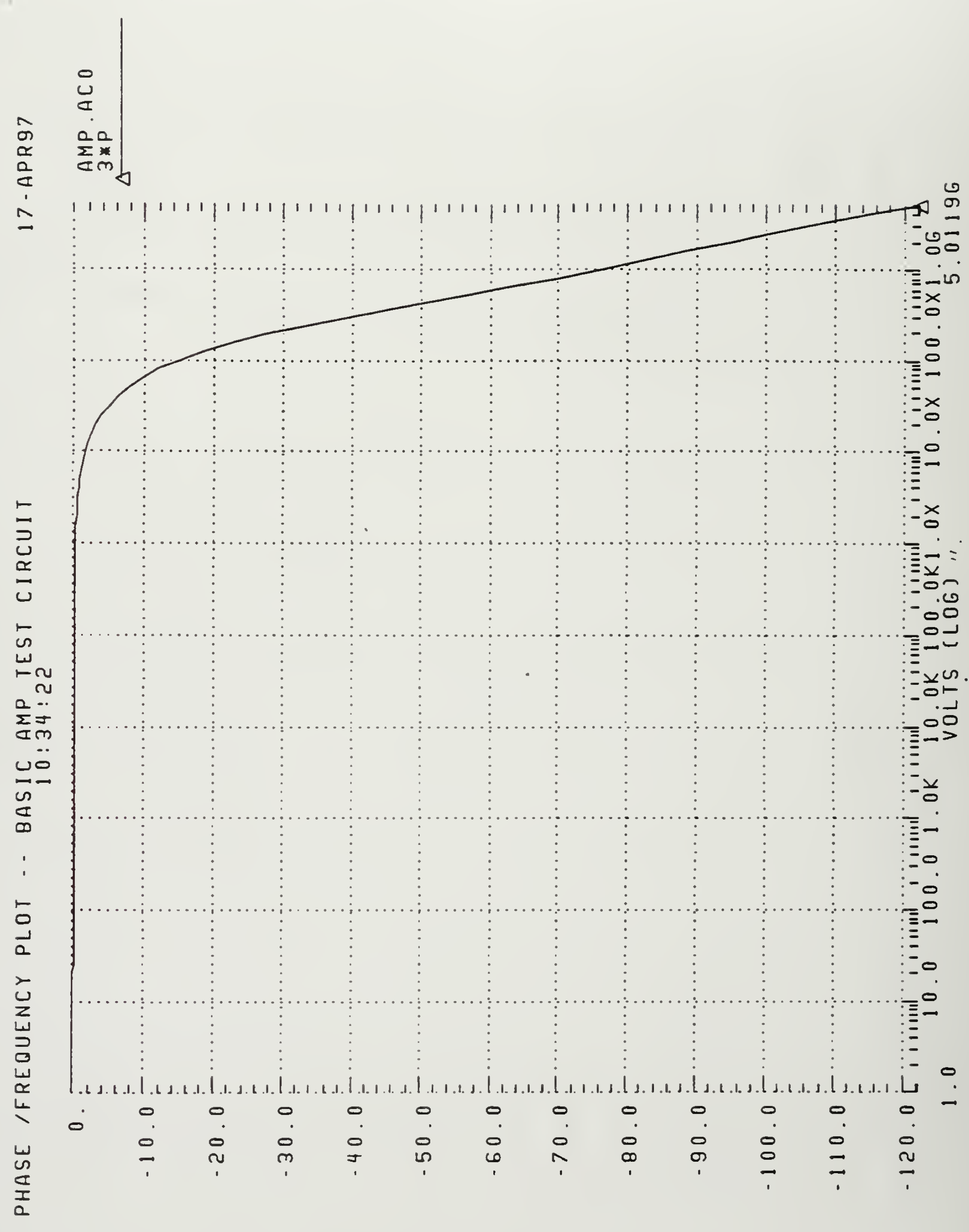
1. Vos Test



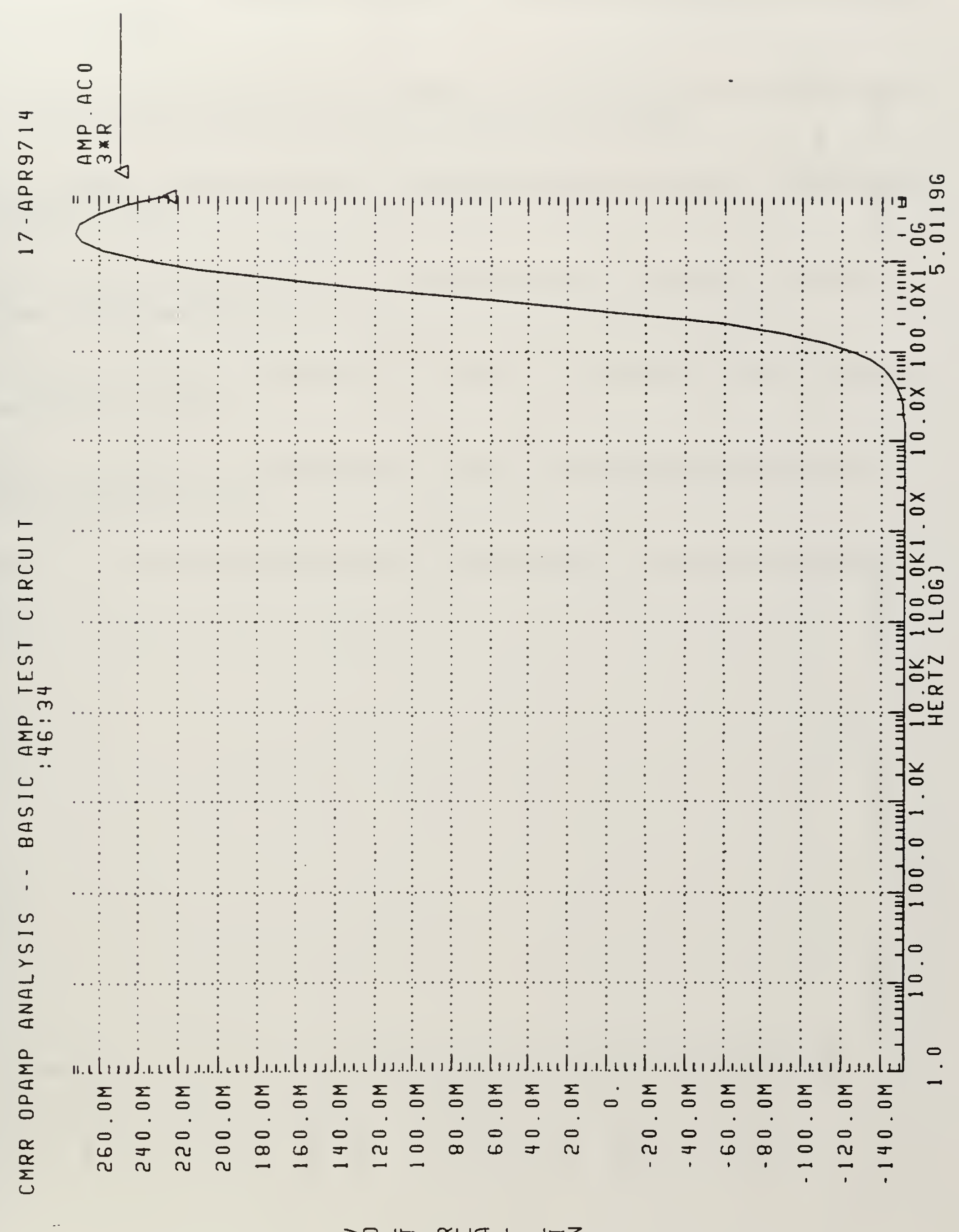
2. Open Loop Gain Test



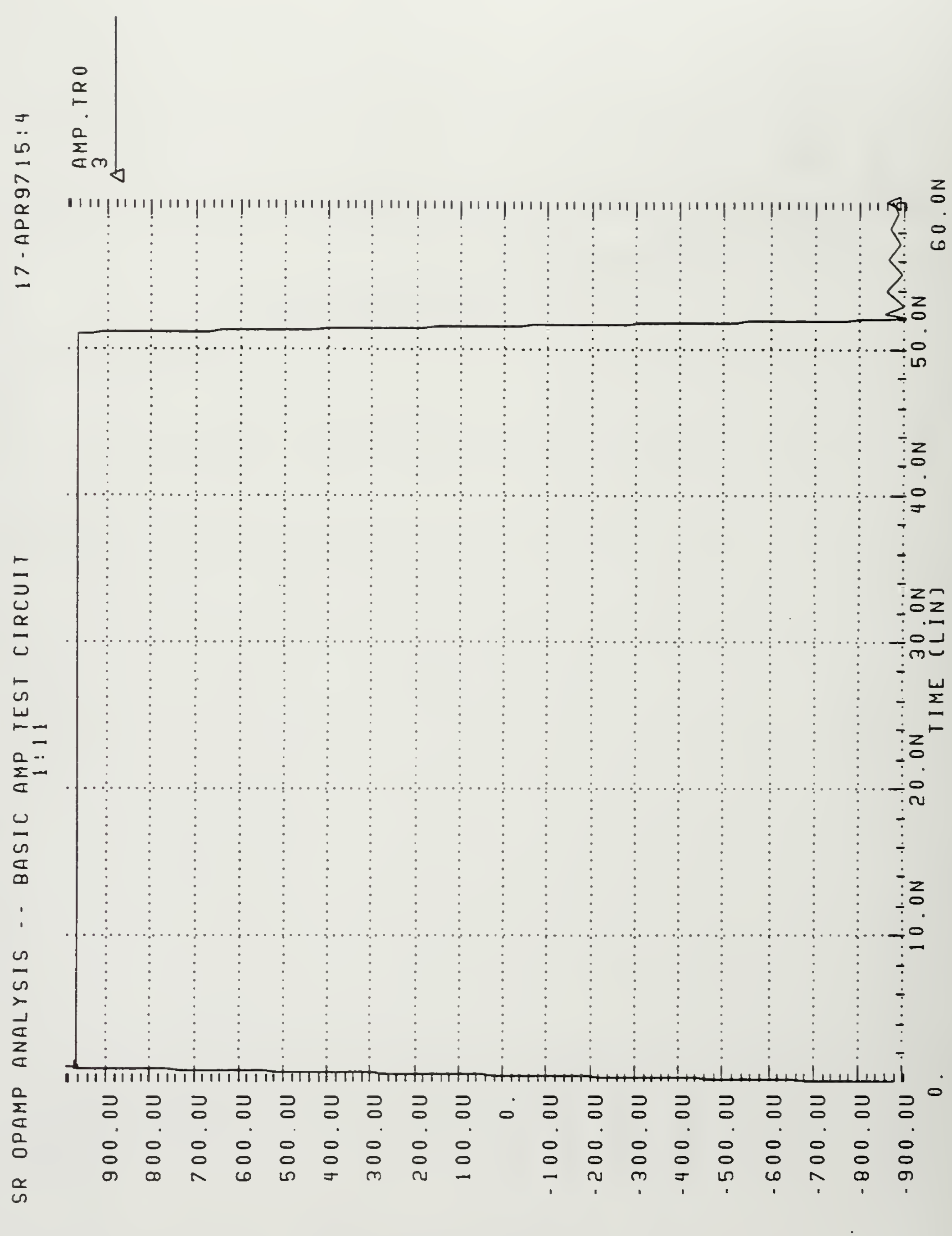
3. Phase Delay Test



4. Common Mode Rejection Ratio Test



5. Slew Rate Test



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